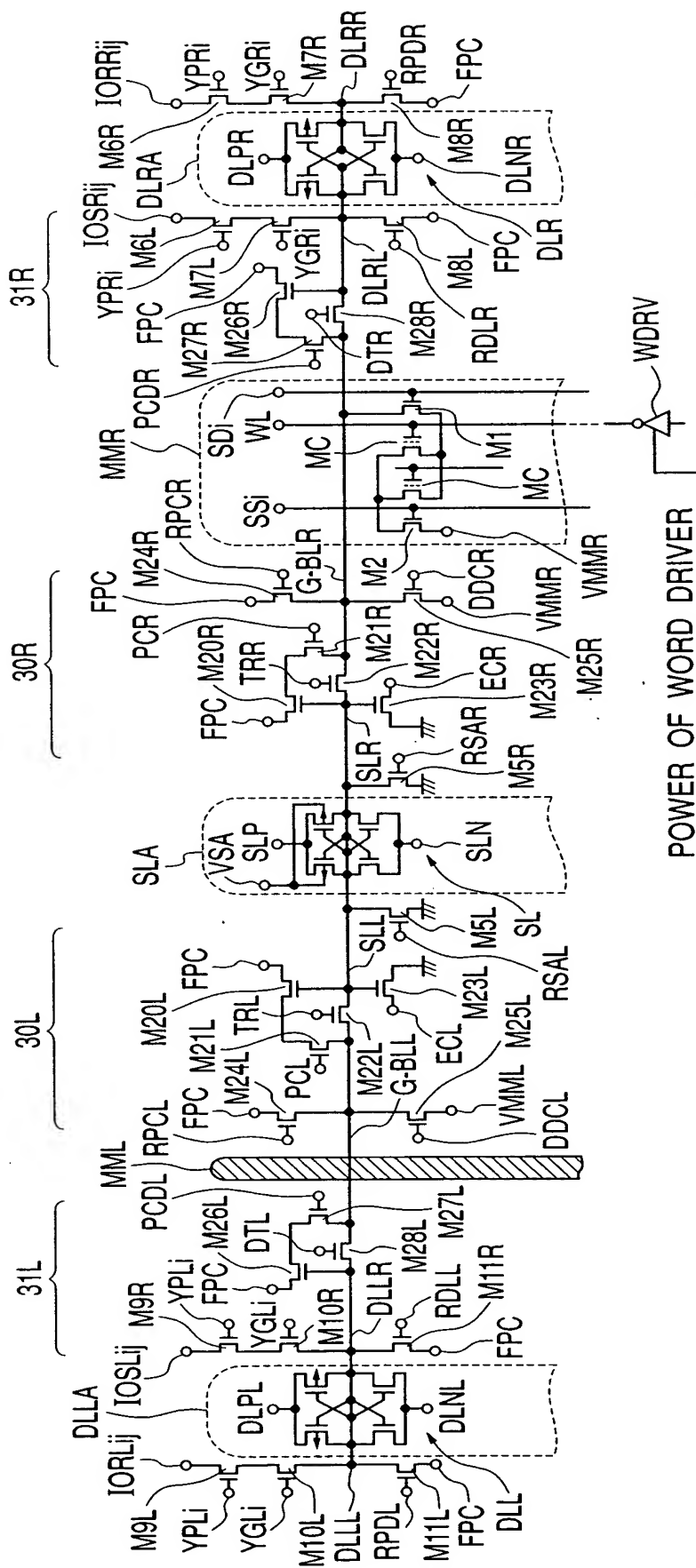


FIG. 1



POWER OF WORD DRIVER

VRW1 THROUGH 3 (READ VOLTAGE)

VWW (WRITE VOLTAGE)

VWV0 THROUGH 3 (WRITE VERIFY VOLTAGE)

VWE1 AND 2 (WRITE ERRATIC DETECTING VOLTAGE)

VWDS (WRITE DISTURB DETECTING VOLTAGE)

VIEW (ERASE VOLTAGE)

VEV (ERASE VERIFY VOLTAGE)

FIG. 2

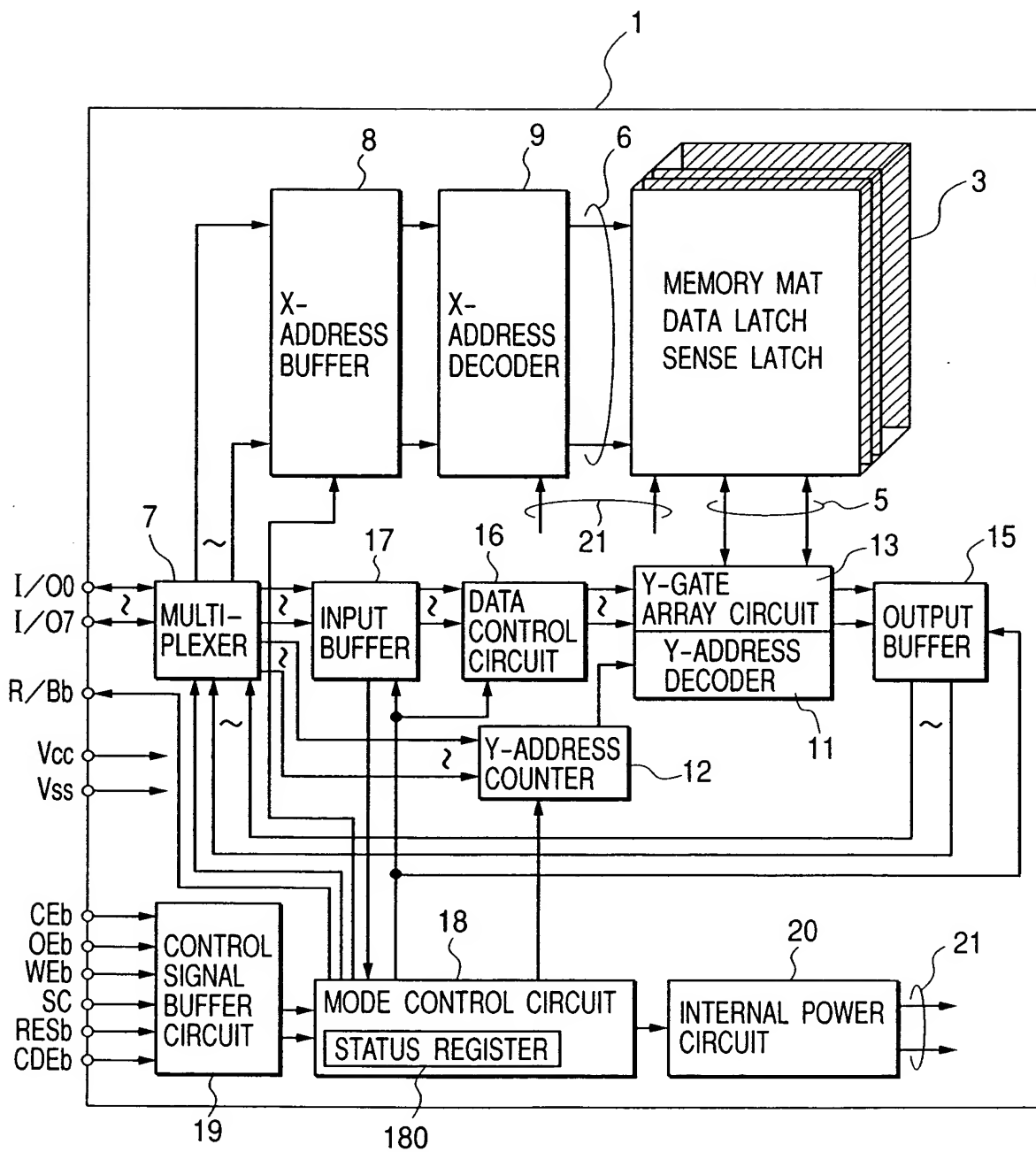
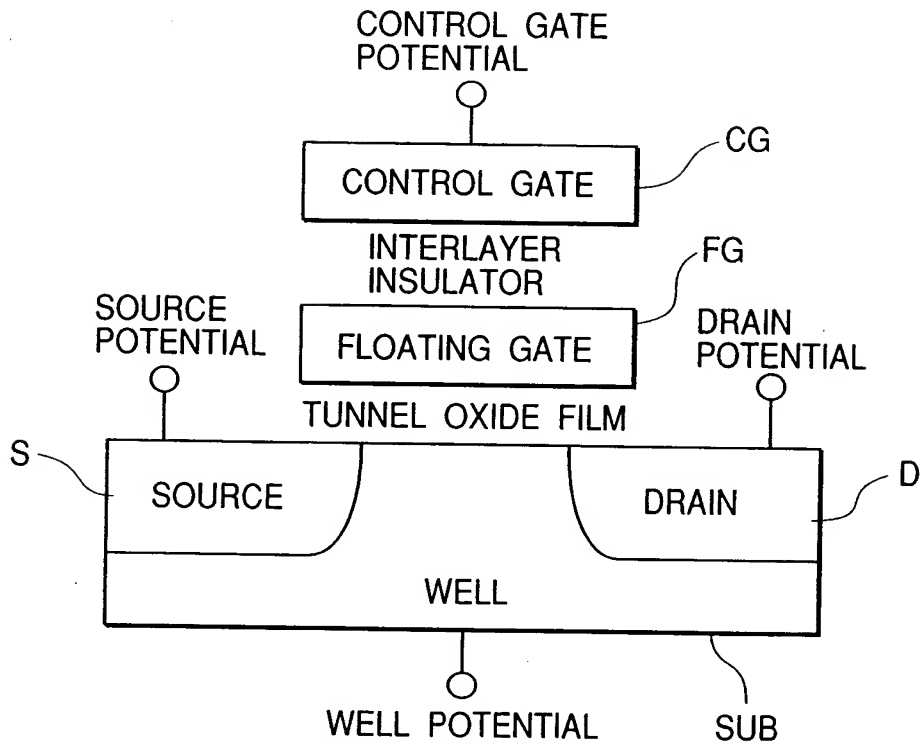


FIG. 3**FIG. 4**

| OPERATING MODE | COMMAND |
|------------------|---------|
| READ | 00H |
| WRITE | 1FH |
| ADDITIONAL WRITE | 10H |
| ERASE | 20H |

FIG. 5

| | DESIGNATION | DEFINITION |
|------|---------------------------------|------------------------|
| I/O7 | Ready/ $\overline{\text{Busy}}$ | "VOH"=Ready "VOL"=Busy |
| I/O6 | Reserved | |
| I/O5 | Erase Check | "VOH"=Fail "VOL"=Pass |
| I/O4 | Program Check | "VOH"=Fail "VOL"=Pass |
| I/O3 | Reserved | |
| I/O2 | Reserved | |
| I/O1 | Reserved | |
| I/O0 | Reserved | |

STATUS REGISTER

FIG. 6

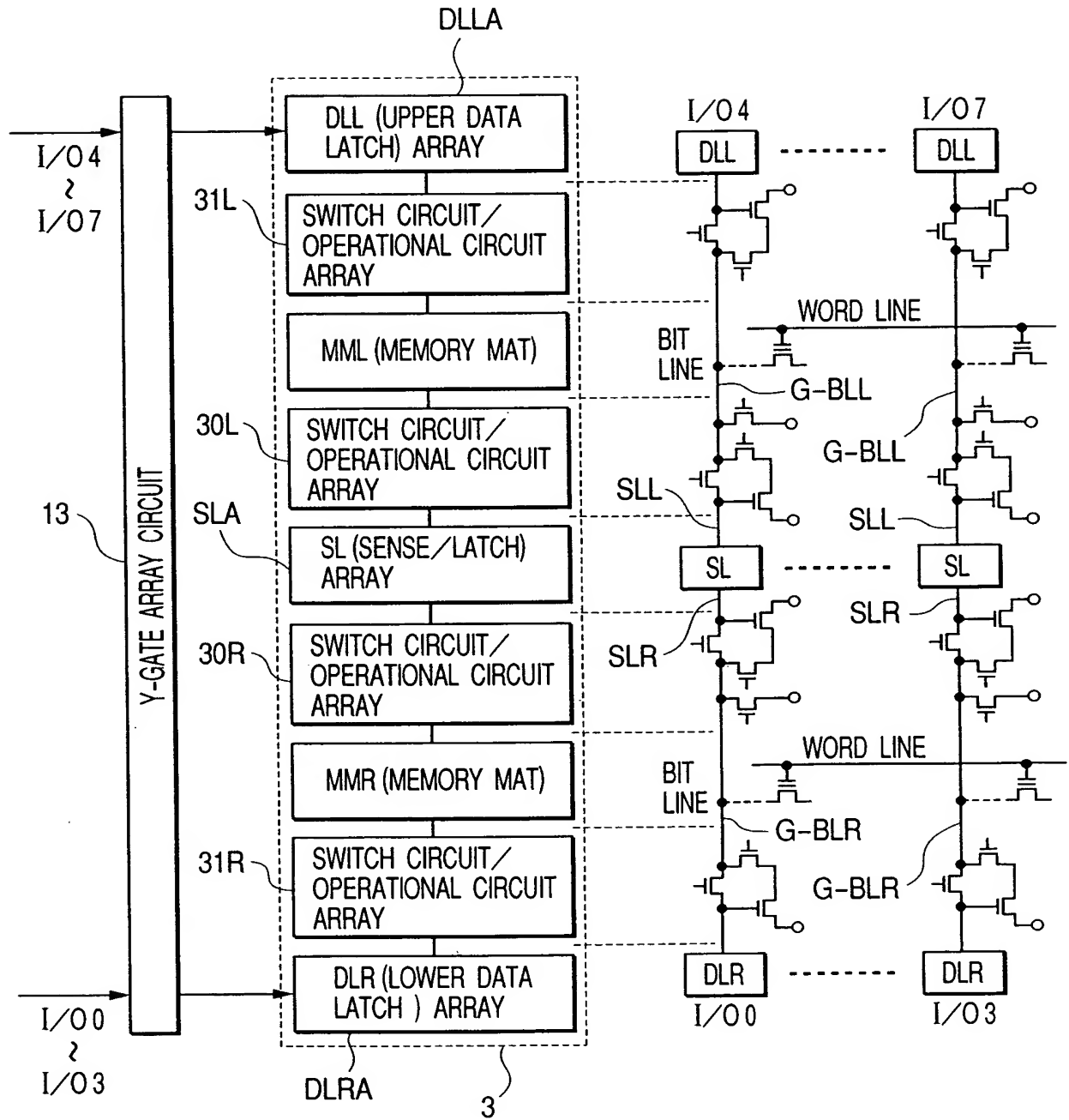


FIG. 7

| WRITE DATA | I/O | | DLL | DLR |
|---------------|-----|---|-----|-----|
| | 4 | 0 | | |
| 01 | 0 | 1 | 0 | 1 |
| 00 | 0 | 0 | 0 | 0 |
| 10 | 1 | 0 | 1 | 0 |
| 11 | 1 | 1 | 1 | 1 |

INPUT WRITE DATA

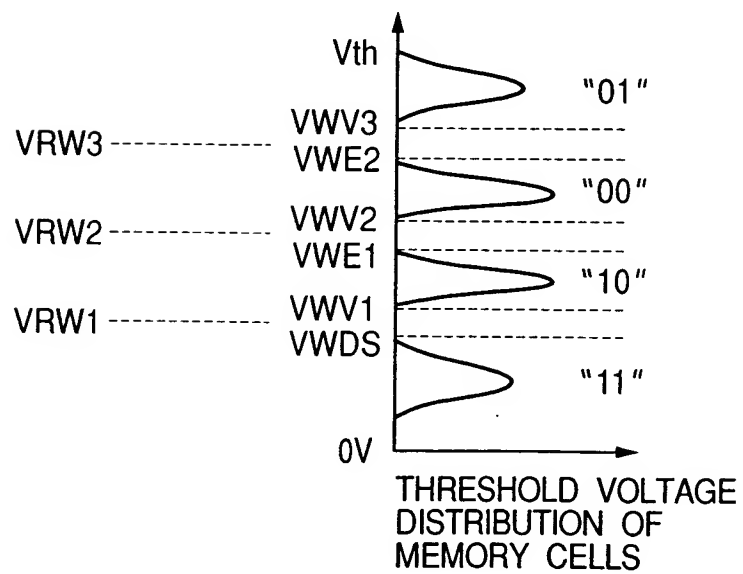
FIG. 8

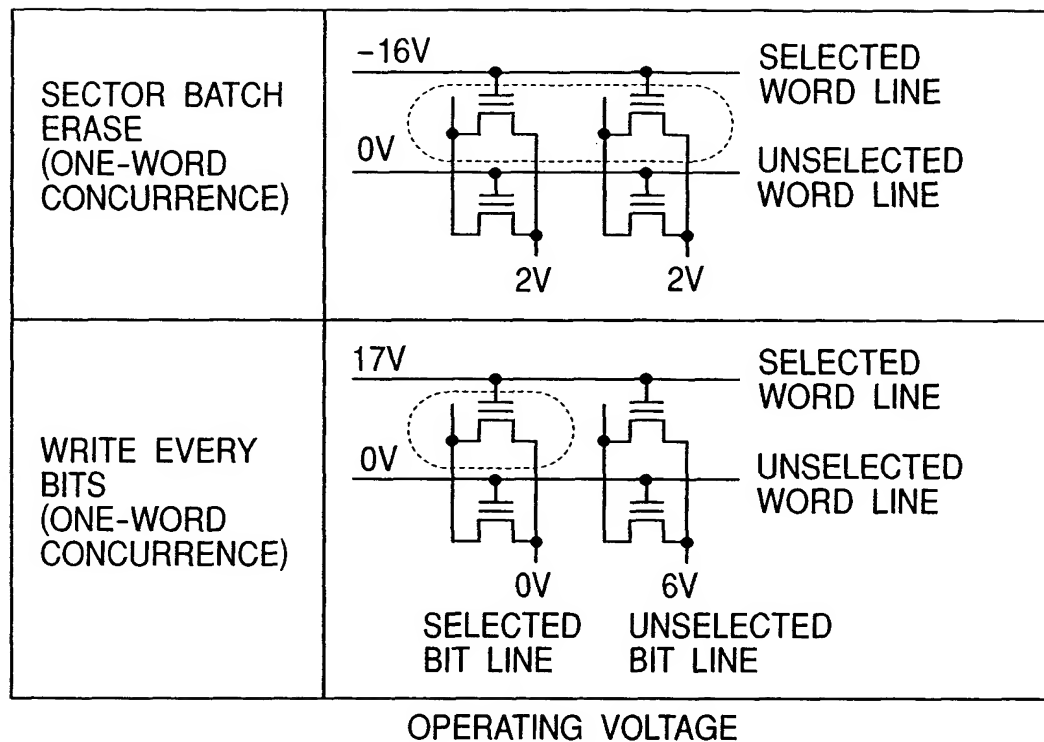
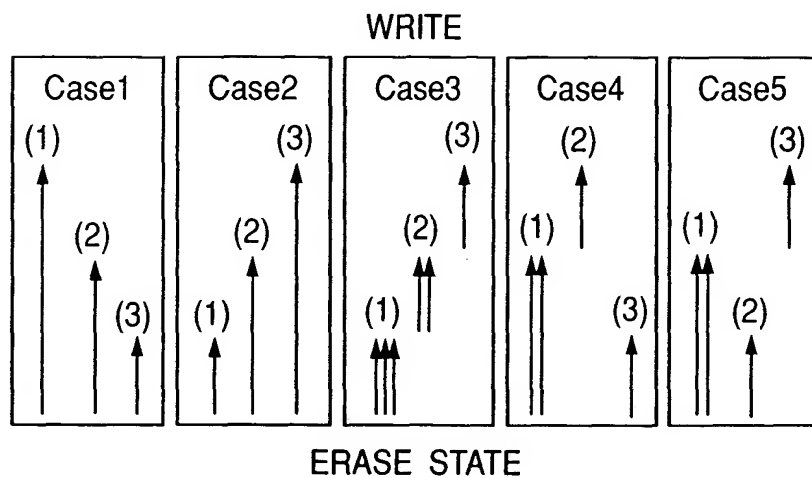
FIG. 9**FIG. 10**

FIG. 11

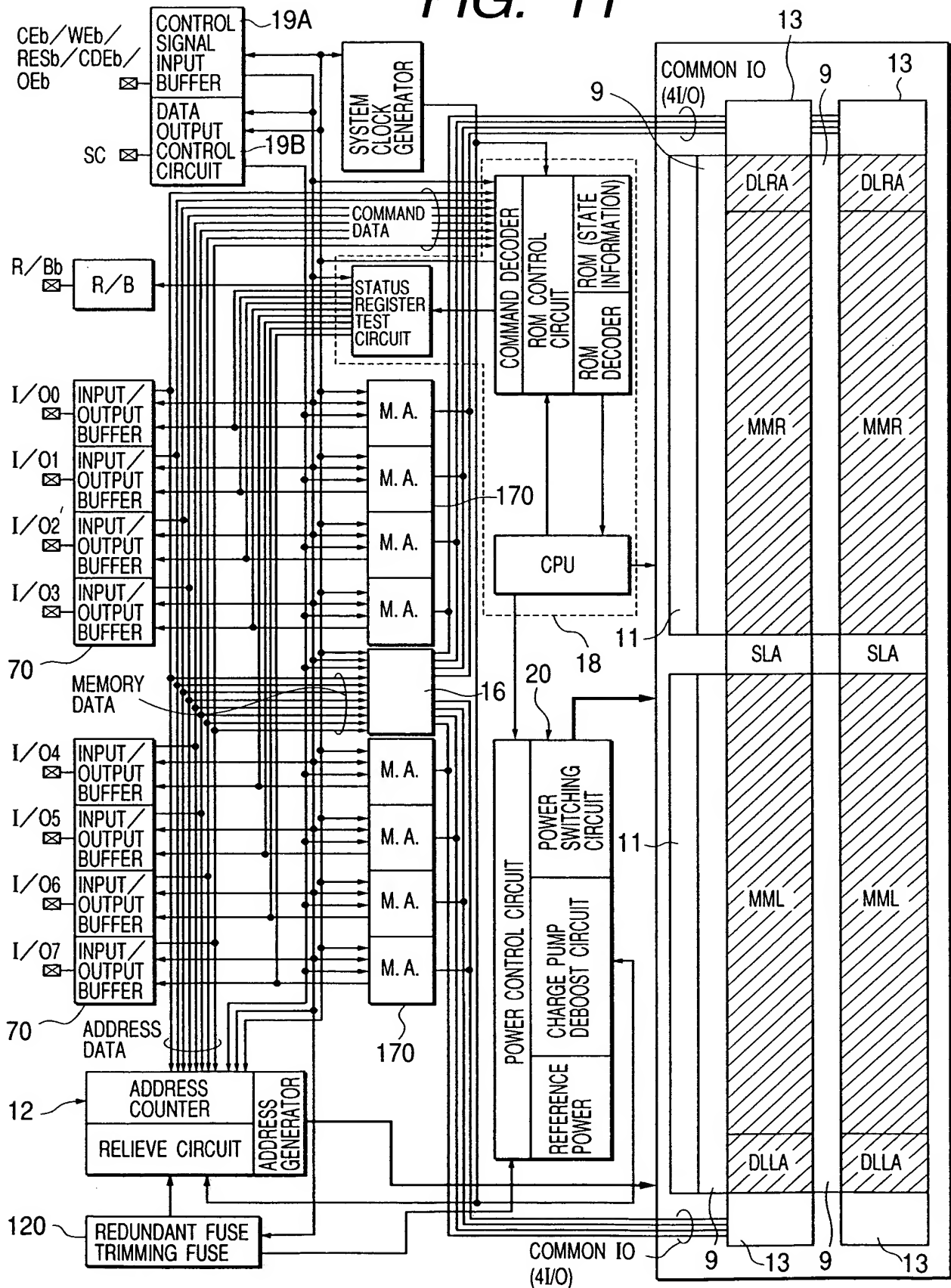


FIG. 12

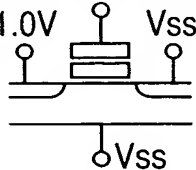
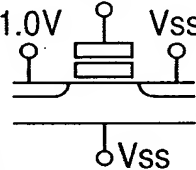
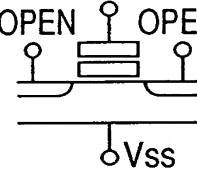
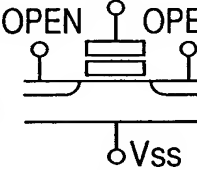
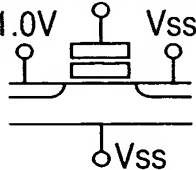
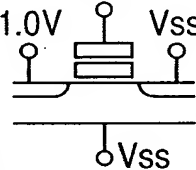
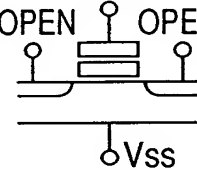
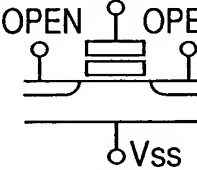
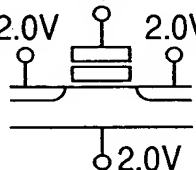
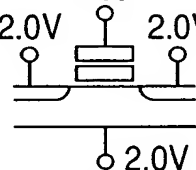
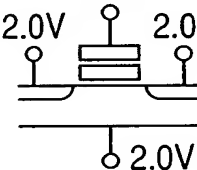
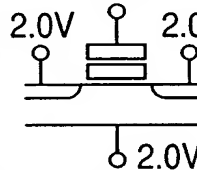
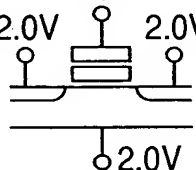
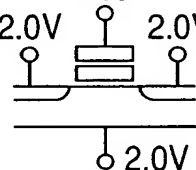
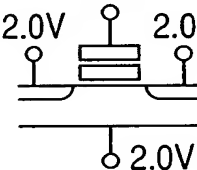
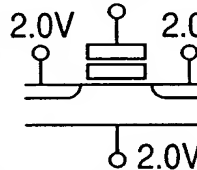
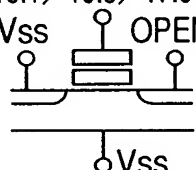
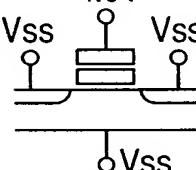
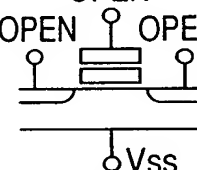
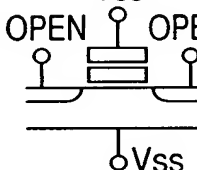
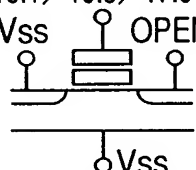
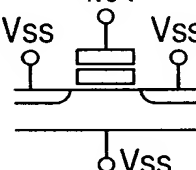
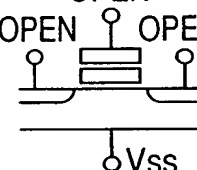
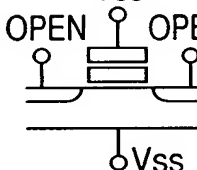
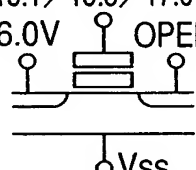
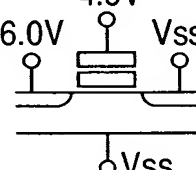
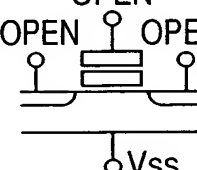
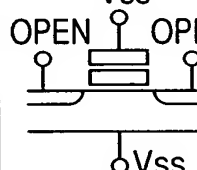
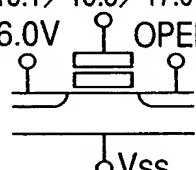
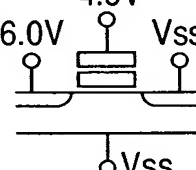
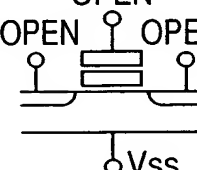
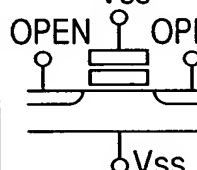
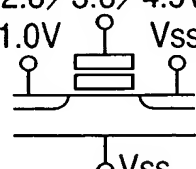
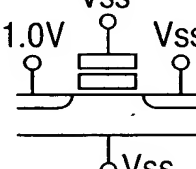
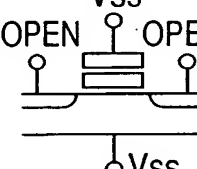
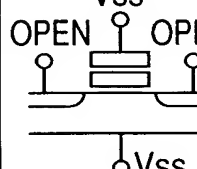
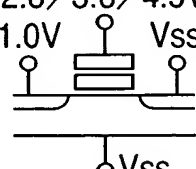
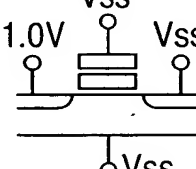
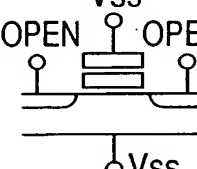
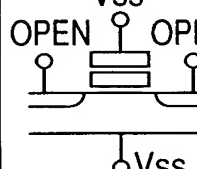
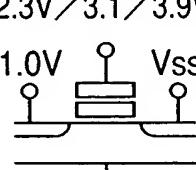
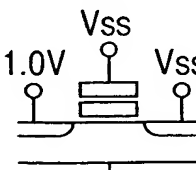
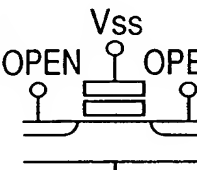
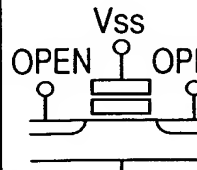
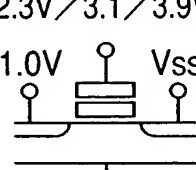
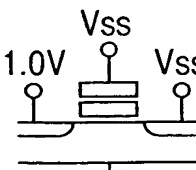
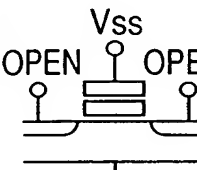
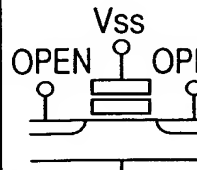
| | | SELECTED BLOCK | | UNSELECTED BLOCK | |
|-------|--|---|---|---|---|
| | | SELECTED WORD | UNSELECTED WORD | SELECTED WORD | UNSELECTED WORD |
| READ | | 2.4/3.2/4.0V 1.0V Vss  | Vss 1.0V Vss  | Vss OPEN OPEN  | Vss OPEN OPEN  |
| | |  |  |  |  |
| ERASE | | -16V 2.0V 2.0V  | Vss 2.0V 2.0V  | 2.0V 2.0V 2.0V  | 2.0V 2.0V 2.0V  |
| | |  |  |  |  |
| WRITE | WRITE DATA | 15.1/15.8/17.0V Vss OPEN  | 4.5V Vss Vss  | OPEN OPEN OPEN  | Vss OPEN OPEN  |
| | |  |  |  |  |
| | NON-WRITE DATA | 15.1/15.8/17.0V 6.0V OPEN  | 4.5V 6.0V Vss  | OPEN OPEN OPEN  | Vss OPEN OPEN  |
| | |  |  |  |  |
| | VERIFY | 2.8/3.6/4.5V 1.0V Vss  | Vss 1.0V Vss  | Vss OPEN OPEN  | Vss OPEN OPEN  |
| | |  |  |  |  |
| | ERRATIC DETECTION DISTURB DETECTION | 2.3V/3.1/3.9V 1.0V Vss  | Vss 1.0V Vss  | Vss OPEN OPEN  | Vss OPEN OPEN  |
| | |  |  |  |  |

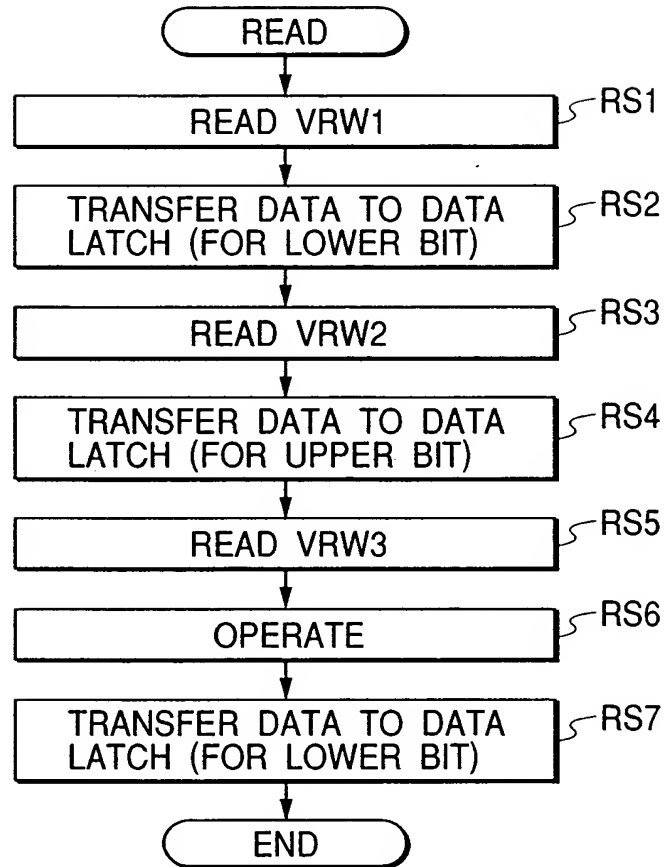
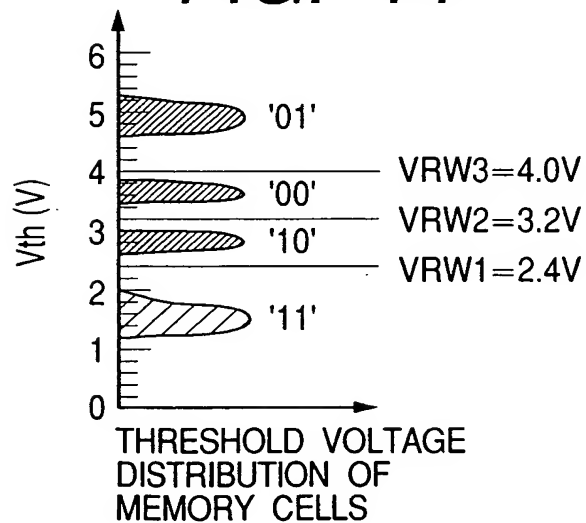
FIG. 13**FIG. 14**

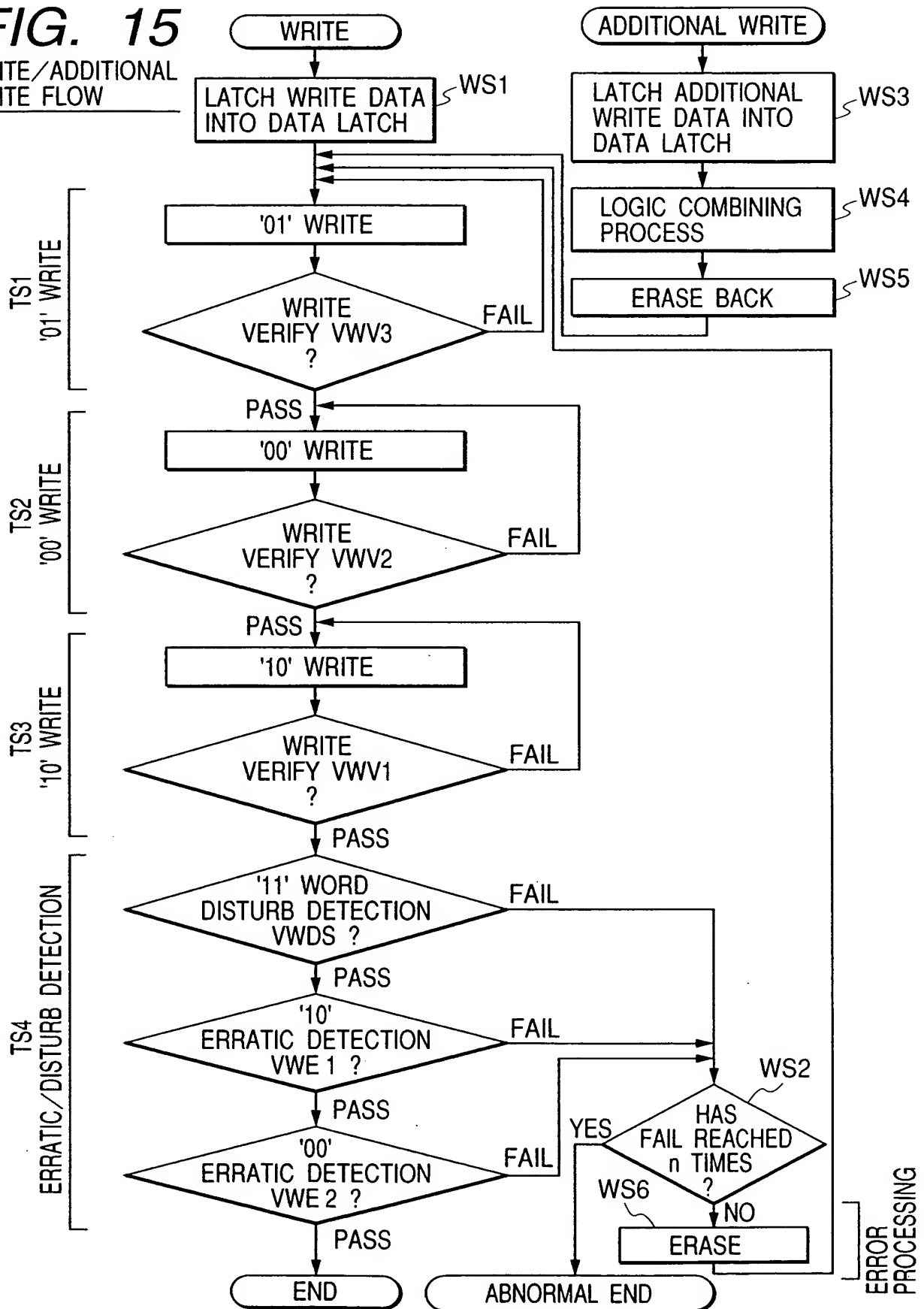
FIG. 15WRITE/ADDITIONAL
WRITE FLOW

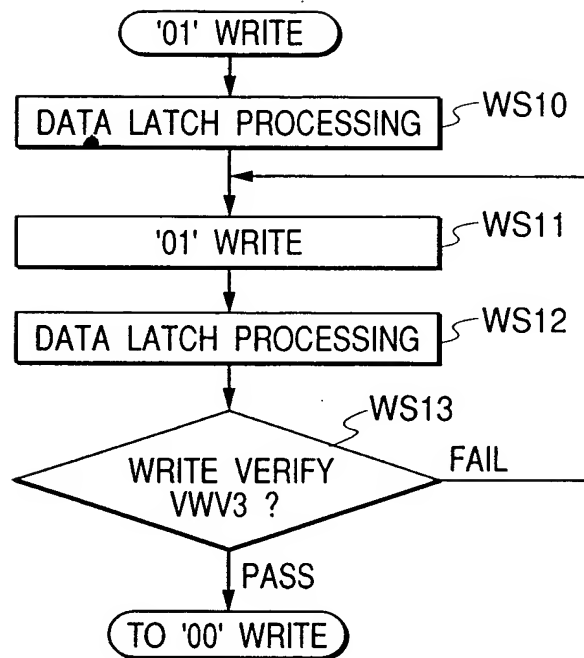
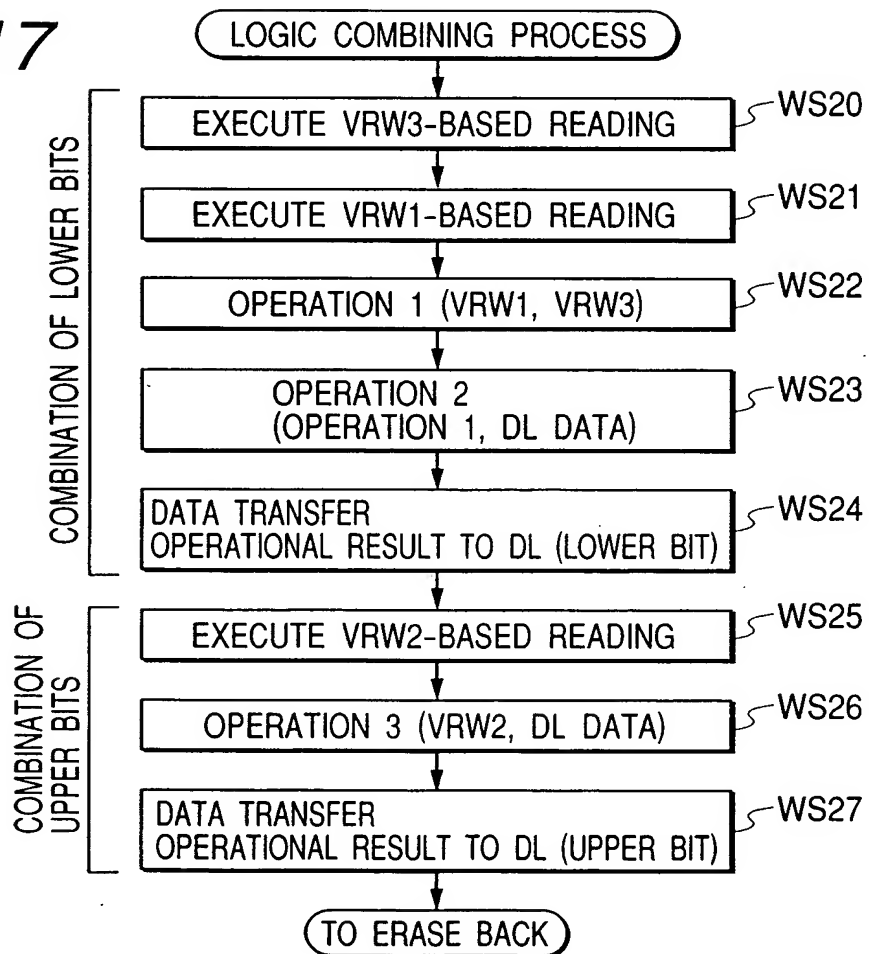
FIG. 16**FIG. 17**

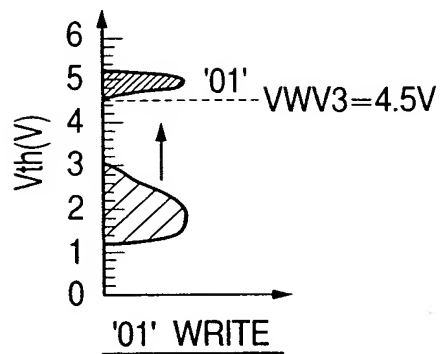
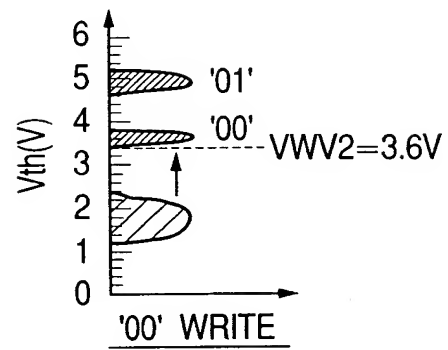
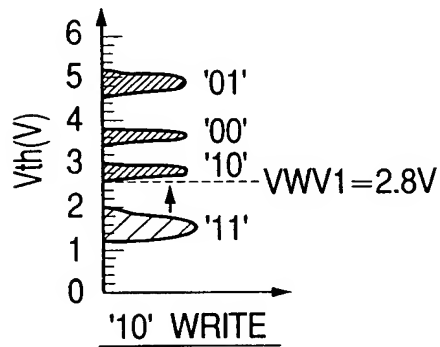
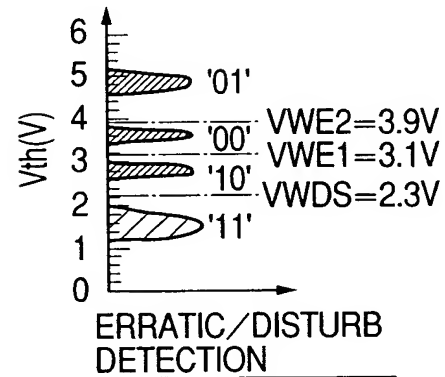
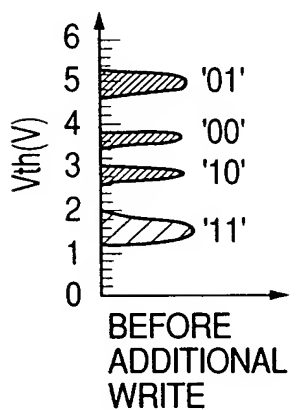
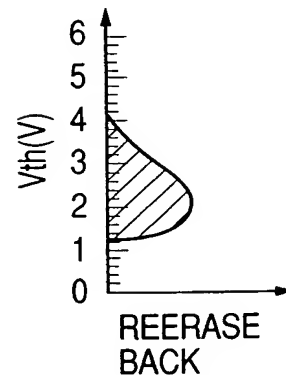
FIG. 18(A)**FIG. 18(B)****FIG. 18(C)****FIG. 18(D)****FIG. 18(E)****FIG. 18(F)**

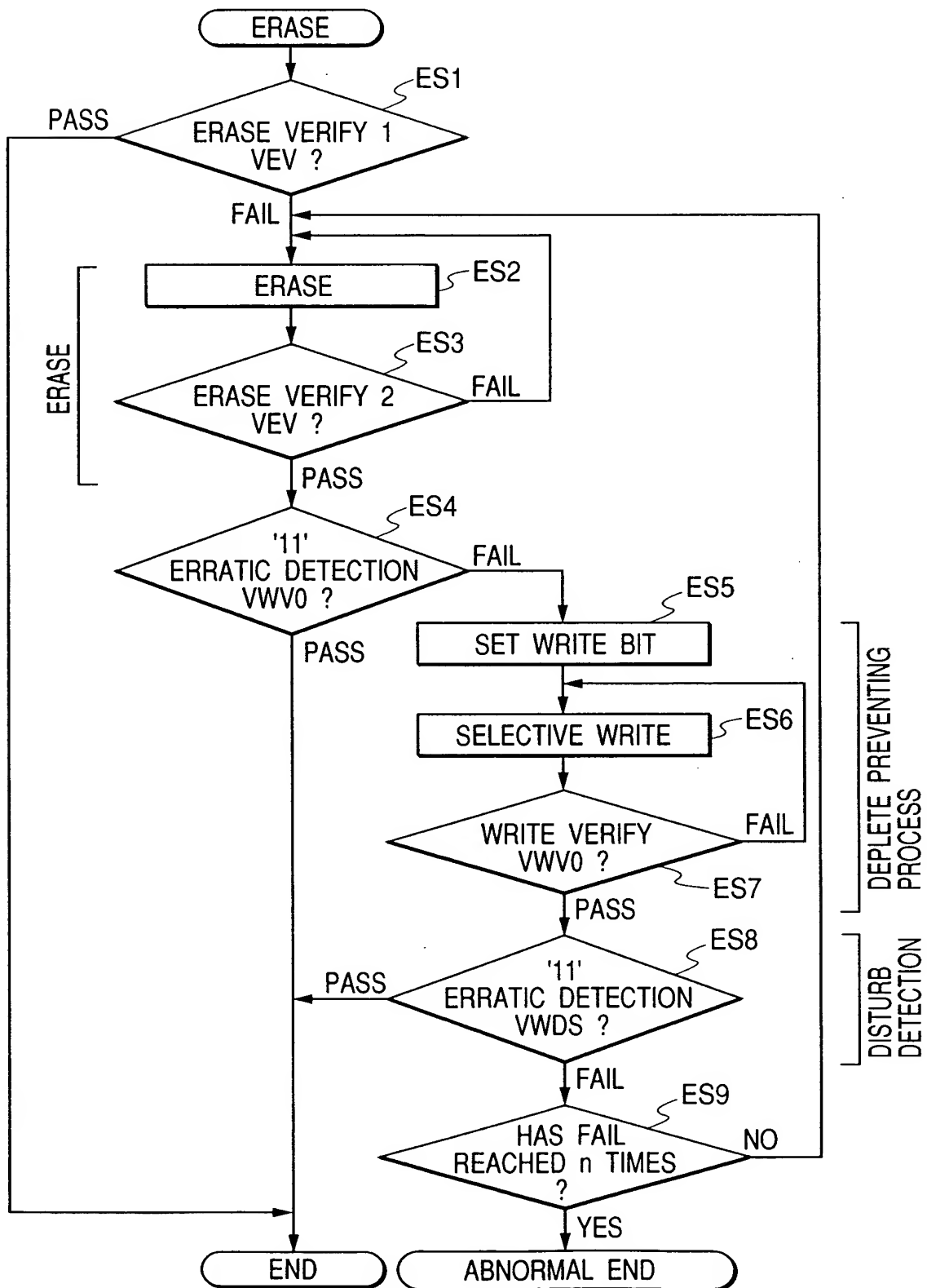
FIG. 19ERASE FLOW

FIG. 20(A)

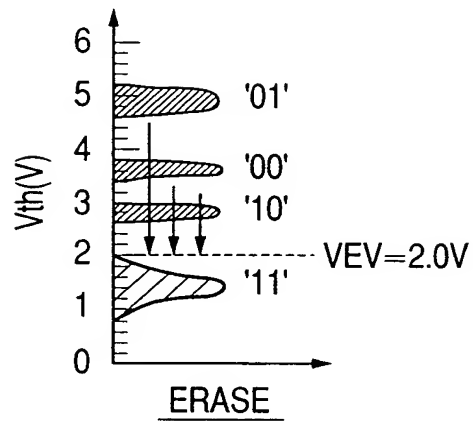


FIG. 20(B)

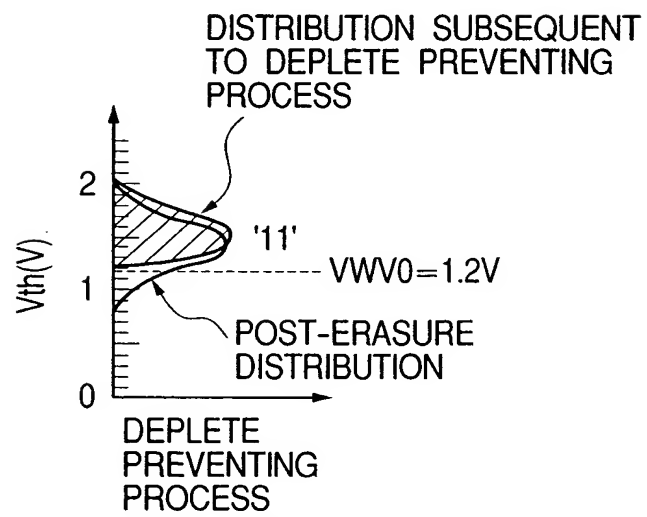


FIG. 21

| DATA LATCH PROCESSING | CONTENTS OF OPERATION (SENSE LATCH DATA ON SELECTED MAT SIDE) |
|-----------------------------|---|
| "01" WRITE DATA | $A + \bar{B}$ |
| "00" WRITE DATA | $A + B$ |
| "10" WRITE DATA | $\bar{A} + B$ |
| "00" ERRATIC DETECTION DATA | $\overline{A + B}$ |
| "10" ERRATIC DETECTION DATA | $A \cdot \bar{B}$ |
| "11" DISTURB DETECTION DATA | $A \cdot B$ |

A : UPPER DATA B : LOWER DATA

FIG. 22

| A UPPER | B LOWER | $A + \bar{B}$ | $A + B$ | $\bar{A} + B$ | $\overline{A + B}$ | $A \cdot \bar{B}$ | $A \cdot B$ |
|------------|------------|---------------|---------|---------------|--------------------|-------------------|-------------|
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

CONCEPT OF ADDITIONAL WRITING

FIG. 23(A)

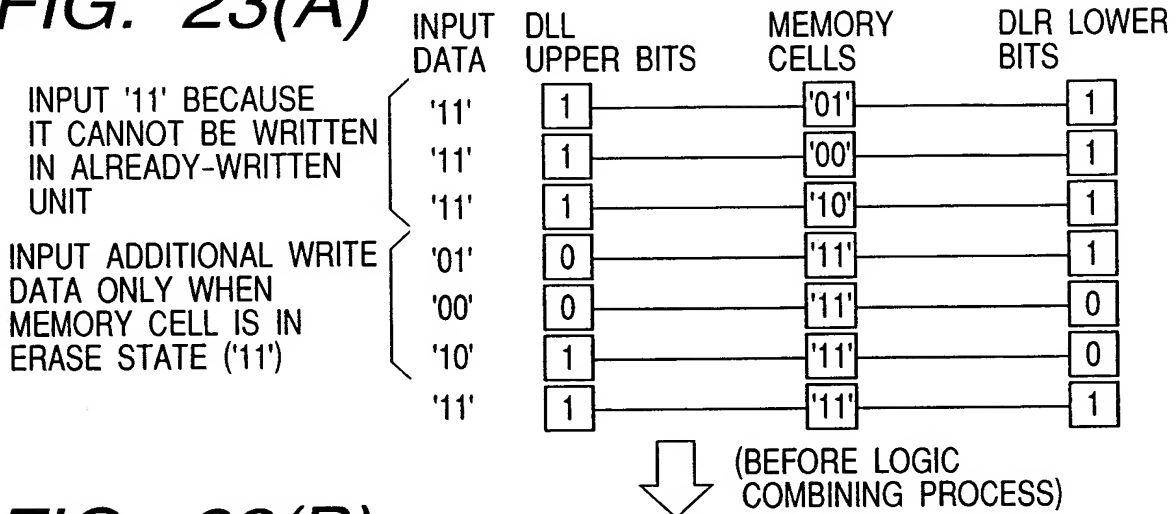


FIG. 23(B)

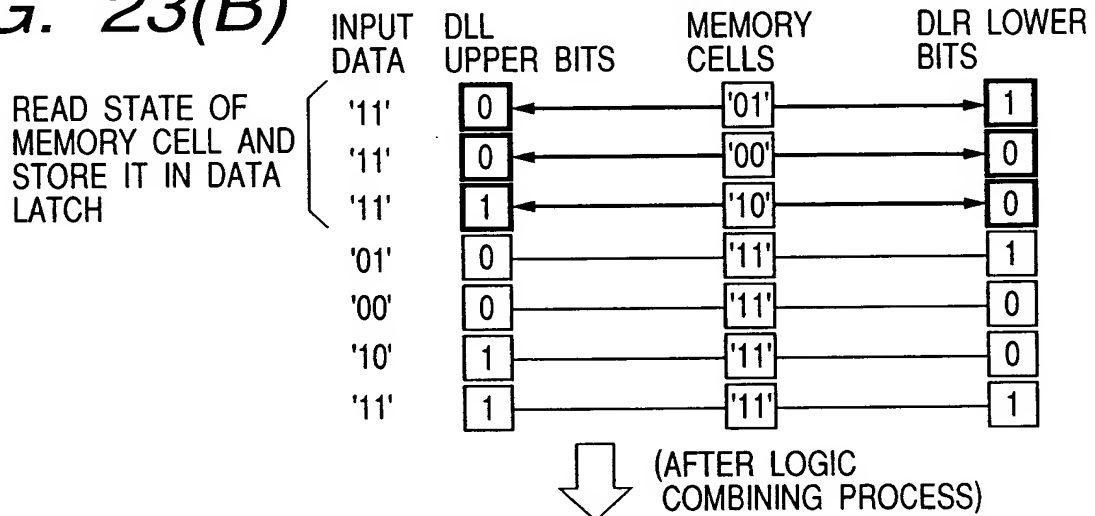


FIG. 23(C)

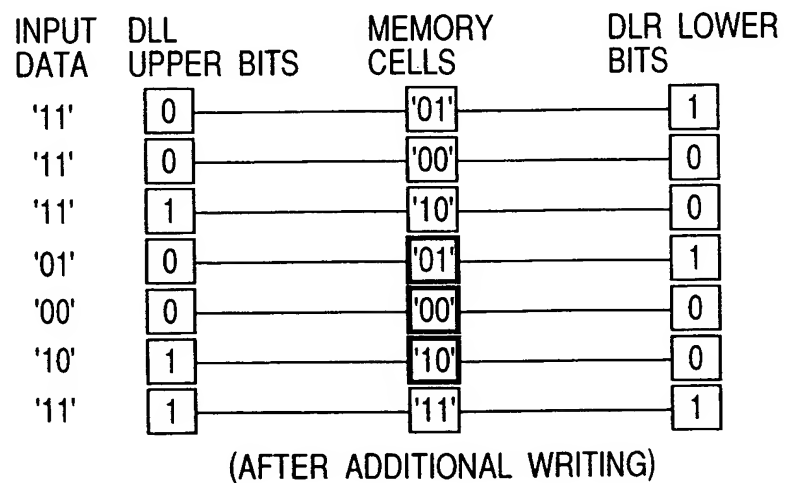


FIG. 24

LOWER BIT : $a0 \cdot \overline{(b1 \oplus b3)}$

UPPER BIT : $\overline{a1} \oplus \overline{b2}$

a0 : ADDITIONAL WRITE DATA (LOWER BIT)

a1 : ADDITIONAL WRITE DATA (UPPER BIT)

b1 : MEMORY READ DATA (VRW1 (2.4V) READ)

b2 : MEMORY READ DATA (VRW2 (3.2V) READ)

b3 : MEMORY READ DATA (VRW3 (4.0V) READ)

\oplus : EXCLUSIVE OR

| STATE OF MEMORY CELL | ADDITIONAL WRITE DATA | a1 | a0 | b1 | b2 | b3 |
|----------------------------|--------------------------|----|----|----|----|----|
| 01 | 11 | 1 | 1 | 1 | 1 | 1 |
| 00 | 11 | 1 | 1 | 1 | 1 | 0 |
| 10 | 11 | 1 | 1 | 1 | 0 | 0 |
| 11 | 01 | 0 | 1 | 0 | 0 | 0 |
| 11 | 00 | 0 | 0 | 0 | 0 | 0 |
| 11 | 10 | 1 | 0 | 0 | 0 | 0 |
| 11 | 11 | 1 | 1 | 0 | 0 | 0 |

FIG. 25

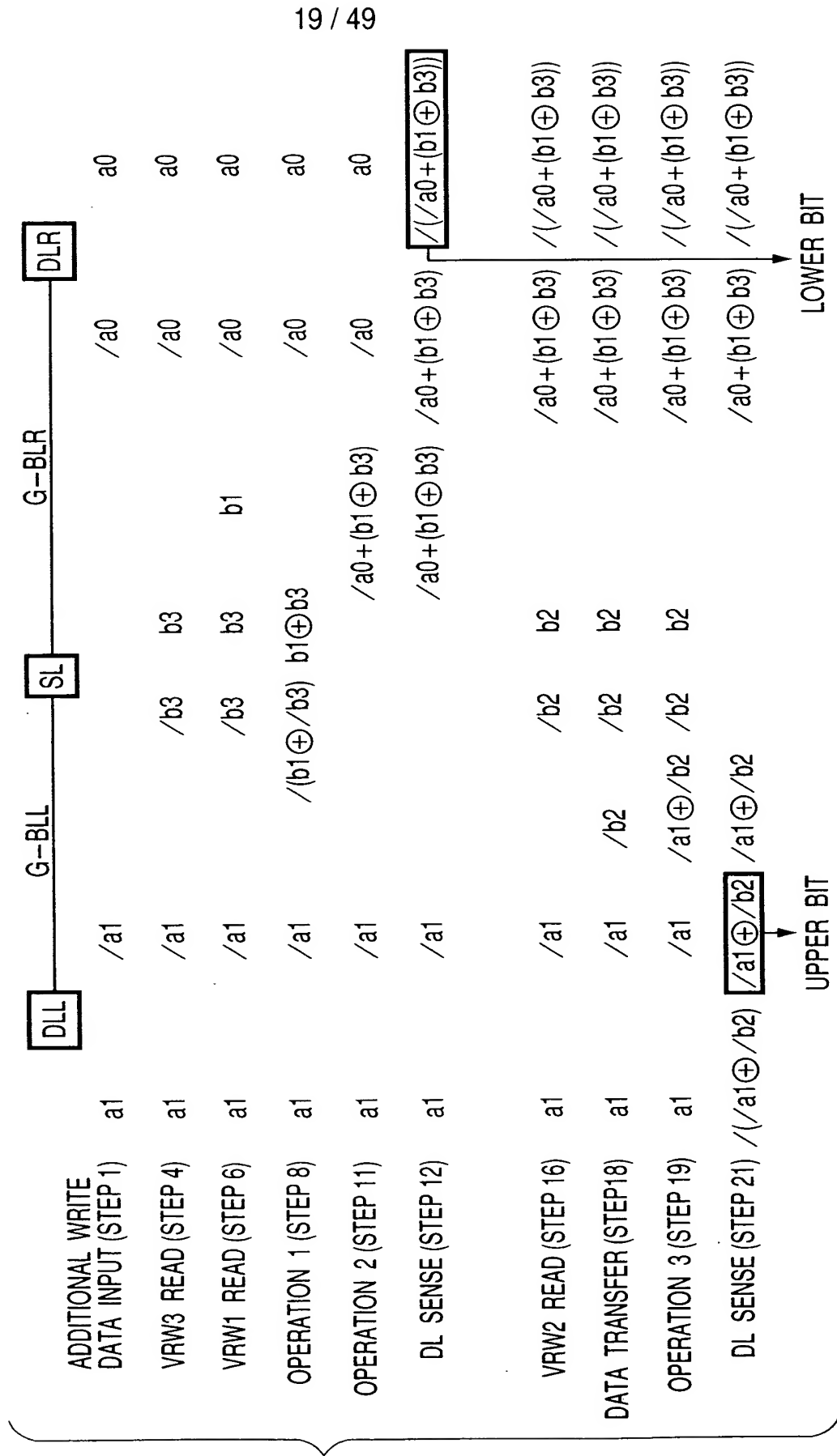


FIG. 27

WRITE SEQUENCE
(1) '01' WRITE

| | | '01' WRITE DATA LATCH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|------------|---|-------|-------|-------|--------|--------------|--------------|-------|----------|-------|-------|-----|---|-------|-------|-------|---------------------------------------|-----|-----|-------|-----------------|-------|-------|-----|----------|-------|-------|-------|-------|-----|--|--|-----|--|--|--|-----|--|--|--|
| STEP | DATA INPUT | STEP 2 | | | | STEP 3 | | | | STEP 4 | | | | STEP 5 | | | | STEP 6 | | | | STEP 7 | | | | | | | | | | | | | | | | | | | |
| CONTENTS | STEP 1 | DATA TRANSFER DRL → G-BLR G-BLL PRECHARGE | | | | | | | | SL SENSE | | | | G-BLL/R DISCHARGE DATA TRANSFER SL(L) → G-BLL | | | | OPERATION (DLL, G-BLL) SL CLEAR | | | | G-BLR PRECHARGE | | | | SL SENSE | | | | | | | | | | | | | | | |
| | | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | | | | | | | | | | |
| | 01 | (1)0 | | | | | (0)1(1)0 0.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 00 | (1)0 | | | | | (1)0(1)0 0.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 10 | (0)1 | | | | | | (1)0(0)1 0.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | (0)1 | | | | | | (0)1(0)1 0.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | (a) | | | | (b) | | | | (c) | | | | (d) | | | | (e) | | | | (f) | | | | (g) | | | | (h) | | | | (i) | | | | (j) | | | |

| '01' WRITE VERIFY | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|-------|--|-------|-------|------|-------------------------------|-------|-------|-------|-------------------------------|------|------|-------|---|-------|-------|------|----------------------------------|-------|-------|-------|-------|------|------|----|---|-----|------|
| STEP 8 | | STEP 9 | | | | STEP 10 | | | | STEP 11 | | | | STEP 12 | | | | STEP 13 | | | | | | | | | | |
| WRITE | | G-BLL/R DISCHARGE G-BLL/R PRECHARGE | | | | MEMORY DISCHARGE (VWV3) | | | | UNSELECTED G-BLR PRECHARGE | | | | SL CLEAR SL SENSE & ALL DETERMINATION | | | | G-BLL/R DISCHARGE SL CLEAR | | | | | | | | | | |
| DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | | | | | |
| (1)0 | 60 | 60 | 00 | 00 | (01) | (1)0 | 05 | 1 | 0 | 1.0 | (01) | (1)0 | 05 | 1 | 0 | 1.0 | (01) | (1)0 | 05 | 0 | 1 | 1.0 | (01) | (1)0 | 00 | 0 | 0.0 | (01) |
| (1)0 | 00 | 00 | 60 | 60 | (1)0 | (1)0 | 05 | 0 | 1 | 0.0 | (1)0 | (1)0 | 05 | 0 | 1 | 1.0 | (1)0 | (1)0 | 05 | 0 | 1 | 1.0 | (1)0 | (1)0 | 00 | 0 | 0.0 | (1)0 |
| (0)1 | 00 | 00 | 60 | 60 | (1)0 | (0)1 | 05 | 0 | 1 | 0.0 | (1)0 | (0)1 | 05 | 0 | 1 | 1.0 | (1)0 | (0)1 | 05 | 0 | 1 | 1.0 | (1)0 | (0)1 | 00 | 0 | 0.0 | (1)0 |
| (0)1 | 00 | 00 | 60 | 60 | (0)1 | (0)1 | 05 | 0 | 1 | 0.0 | (0)1 | (0)1 | 05 | 0 | 1 | 1.0 | (0)1 | (0)1 | 05 | 0 | 1 | 1.0 | (0)1 | (0)1 | 00 | 0 | 0.0 | (0)1 |

ALL DETERMINATION: TO STEP 8 IF FAIL IS REACHED

FIG. 28

170A: 20

(2) '00' WRITE

| '00' WRITE DATA LATCH | | | | | | | | | | | | | | | | |
|-----------------------|---|-------|-------|---------|-------------------------------|------|-----|---------|--|-------|-------|---------|---|-------|-------|-------|
| STEP | STEP 14 | | | | STEP 15 | | | | STEP 16 | | | | | | | |
| CONTENTS | DATA TRANSFER DRL → G-BLR G-BLL PRECHARGE | | | | SL SENSE | | | | G-BLL/R DISCHARGE G-BLL/R PRECHARGE | | | | | | | |
| | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DRL | DLL | G-BLL | G-BLL | SL(L) | SL(R) | G-BLR | | | | |
| 01 | (1)0.5 | 0.0 | (0)1 | (1)0 | 1 | 1 | 0 | 0 | (0)1 | (1)0 | 1.0 | 1 | | | | |
| 00 | (1)0.5 | 1.0 | (1)0 | (1)0 | 0 | 0 | 1 | 1 | (1)0 | (1)0 | 1.0 | 0 | | | | |
| 10 | (0)1.5 | 1.0 | (1)0 | (0)1 | 0 | 0 | 1 | 1 | (1)0 | (0)1 | 1.0 | 0 | | | | |
| 11 | (0)1.5 | 0.0 | (0)1 | (0)1 | 1 | 1 | 0 | 0 | (0)1 | (0)1 | 1.0 | 1 | | | | |
| '00' WRITE VERIFY | | | | | | | | | | | | | | | | |
| STEP 20 | | | | STEP 21 | | | | STEP 22 | | | | STEP 23 | | | | |
| WRITE | G-BLL/R DISCHARGE G-BLL/R PRECHARGE | | | | MEMORY DISCHARGE (VWV2) | | | | UNSELECTED G-BLR PRECHARGE | | | | SL CLEAR SL SENSE & ALL DETERMINATION | | | |
| | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DRL | DLL | G-BLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) |
| | (1)0.0 | 0.0 | 6.0 | 6.0 | (0)1 | (1)0 | 0.5 | 0 | 1 | 1.0 | (0)1 | (1)0 | 0.5 | 0 | 1 | 1.0 |
| | (1)0.6 | 6.0 | 0.0 | 0.0 | (1)0 | (1)0 | 0.5 | 1 | 0 | 1.0 | (1)0 | 0.5 | 1 | 0 | 1.0 | (1)0 |
| | (0)1.0 | 0.0 | 6.0 | 6.0 | (1)0 | (0)1 | 0.5 | 0 | 1 | 1.0 | (1)0 | 0.5 | 0 | 1 | 1.0 | (1)0 |
| | (0)1.0 | 0.0 | 6.0 | 6.0 | (1)0 | (0)1 | 0.5 | 0 | 1 | 1.0 | (1)0 | 0.5 | 0 | 1 | 1.0 | (1)0 |
| | (0)1.0 | 0.0 | 6.0 | 6.0 | (1)0 | (0)1 | 0.5 | 0 | 1 | 1.0 | (1)0 | 0.5 | 0 | 1 | 1.0 | (1)0 |
| | (0)1.0 | 0.0 | 6.0 | 6.0 | (1)0 | (0)1 | 0.5 | 0 | 1 | 1.0 | (1)0 | 0.5 | 0 | 1 | 1.0 | (1)0 |
| | (0)1.0 | 0.0 | 6.0 | 6.0 | (1)0 | (0)1 | 0.5 | 0 | 1 | 1.0 | (1)0 | 0.5 | 0 | 1 | 1.0 | (1)0 |

ALL DETERMINATION: TO STEP 20 IF FAIL IS REACHED

FIG. 29

[illegible]

ALL DETERMINATION: TO STEP 32 IF FAIL IS REACHED

FIG. 30

(4) '11' WORD DISTURB DETECTION

| '11' WORD DISTURB DATA LATCH | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------|---|---------|-------|-------|----------|---------|-------|-------|--|---------|-------|-------|-----------------------------|---------|-------|-------|---------------------------------------|---------|------|-------|----------|---------|-------|------|------|
| STEP | | STEP 38 | | | | STEP 39 | | | | STEP 40 | | | | STEP 41 | | | | STEP 42 | | | | STEP 43 | | | |
| CONTENTS | DATA TRANSFER DLL → G-BLL G-BLR PRECHARGE | | | | SL SENSE | | | | G-BLL/R DISCHARGE G-BLL/R PRECHARGE | | | | OPERATION (SL(R), G-BLR) | | | | OPERATION (G-BLR, DLR) SL CLEAR | | | | SL SENSE | | | | |
| | DLL | G-BLL | SL(L) | SL(R) | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | |
| | (1)0 | 0.0 | | | 0.5 | (0)1 | (1)0 | 0 | 0 | 1 | 1 | (0)1 | (1)0 | 0.5 | 0 | 1 | 0.0 | (0)1 | (1)0 | 0.5 | 0 | 0 | 0.0 | (0)1 | (1)0 |
| | (1)0 | 0.0 | | | 0.5 | (1)0 | (1)0 | 0 | 0 | 1 | 1 | (1)0 | (1)0 | 0.5 | 0 | 1 | 0.0 | (1)0 | (1)0 | 0.5 | 0 | 0 | 0.0 | (1)0 | (1)0 |
| | 10 | (0)1 | 1.0 | | | 0.5 | (1)0 | (0)1 | 1 | 1 | 0 | 0 | (1)0 | (0)1 | 0.5 | 1 | 0 | 1.0 | (1)0 | (0)1 | 0.5 | 0 | 0 | 0.0 | (1)0 |
| 11 | (0)1 | 1.0 | | | 0.5 | (0)1 | (0)1 | 1 | 1 | 0 | 0 | (0)1 | (0)1 | 0.5 | 1 | 0 | 1.0 | (0)1 | (0)1 | 0.5 | 0 | 0 | 1.0 | (0)1 | (0)1 |

| '11' WORD DISTURB DETECTION | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------------|-------|-------|-------|--|-------|-------|-------|-------------------------------|-------|-------|-------|---|-----|-------|-------|----------------------------------|-------|------|-------|-------|-------|-------|------|
| STEP 44 | | | | STEP 45 | | | | STEP 46 | | | | STEP 47 | | | | STEP 48 | | | | | | | |
| G-BLL/R DISCHARGE | | | | G-BLR SELECT PRECHARGE G-BLL PRECHARGE | | | | MEMORY DISCHARGE (VWDS) | | | | SL CLEAR SL SENSE & ALL DETERMINATION | | | | G-BLL/R DISCHARGE SL CLEAR | | | | | | | |
| DLL | G-BLL | SL(L) | SL(R) | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL |
| (1)0 | 0 | 1 | 0 | 0 | (0)1 | (1)0 | 0.5 | 1 | 0 | 0.0 | (0)1 | (1)0 | 0.5 | 1 | 0 | 0.0 | (0)1 | (1)0 | 0.5 | 0 | 0 | 0.0 | (0)1 |
| (1)0 | 0 | 1 | 0 | 0 | (1)0 | (1)0 | 0.5 | 1 | 0 | 0.0 | (1)0 | (1)0 | 0.5 | 1 | 0 | 0.0 | (1)0 | (1)0 | 0.5 | 0 | 0 | 0.0 | (1)0 |
| (0)1 | 0 | 1 | 0 | 0 | (1)0 | (0)1 | 0.5 | 1 | 0 | 0.0 | (1)0 | (0)1 | 0.5 | 1 | 0 | 0.0 | (1)0 | (0)1 | 0.5 | 0 | 0 | 0.0 | (1)0 |
| (0)1 | 0 | 0 | 1 | 0 | (0)1 | (0)1 | 0.5 | 0 | 1 | 0.0 | (0)1 | (0)1 | 0.5 | 1 | 0 | 0.0 | (0)1 | (0)1 | 0.5 | 0 | 0 | 0.0 | (0)1 |

ALL DETERMINATION: TO ERASE IF FAIL IS REACHED

FIG. 31

(5) '10' ERRATIC DETECTION

| '10' ERRATIC DATA LATCH | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|----------|---|-------|-------|----------|----------|-------|-------|-----------|---|-------|-------|----------|-----------------------------|-------|-------|----------|-----------------------------|-------|-------|----------|----------|-------|-------|--------|--|
| STEP | | STEP 49 | | | | STEP 50 | | | | STEP 51 | | | | STEP 52 | | | | STEP 53 | | | | STEP 54 | | | | |
| CONTENTS | | DATA TRANSFER DLL → G-BLL G-BLR PRECHARGE | | | | SL SENSE | | | | G-BLL/R DISCHARGE DATA TRANSFER DLR → G-BLR | | | | OPERATION (SL(R), G-BLR) | | | | SL CLEAR G-BLL PRECHARGE | | | | SL SENSE | | | | |
| | | DLL | G-BLL | SL(L) | SL(R) | DLL | G-BLL | SL(L) | SL(R) | DLL | G-BLL | SL(L) | SL(R) | DLL | G-BLL | SL(L) | SL(R) | DLL | G-BLL | SL(L) | SL(R) | DLL | G-BLL | SL(L) | SL(R) | |
| | | DLR | G-BLR | | | DLR | G-BLR | | | DLR | G-BLR | | | DLR | G-BLR | | | DLR | G-BLR | | | DLR | G-BLR | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 | (1)0 0.0 | | | | 0.5 (0)1 | (1)0 0 | 0 | 1 | (0)1 (1)0 | 0 | 0 | 1 | 0.0 (0)1 | (1)0 0 | 0 | 1 | 0.0 (0)1 | (1)0 0.5 | 0 | 0 | 0.0 (0)1 | (1)0 1 | 1 | 0 | 0 (0)1 | |
| 00 | (1)0 0.0 | | | | 0.5 (1)0 | (1)0 0 | 0 | 1 | (1)0 (1)0 | 0 | 0 | 1 | 1.0 (1)0 | (1)0 0 | 0 | 1 | 0.0 (1)0 | (1)0 0.5 | 0 | 0 | 0.0 (1)0 | (1)0 1 | 1 | 0 | 0 (1)0 | |
| 10 | (0)1 1.0 | | | | 0.5 (1)0 | (0)1 1 | 1 | 0 | (1)0 (0)1 | 0 | 1 | 0 | 1.0 (1)0 | (0)1 0 | 1 | 0 | 1.0 (1)0 | (0)1 0.5 | 0 | 0 | 1.0 (1)0 | (0)1 0 | 0 | 1 | 1 (1)0 | |
| 11 | (0)1 1.0 | | | | 0.5 (0)1 | (0)1 1 | 1 | 0 | (0)1 (0)1 | 0 | 1 | 0 | 0.0 (0)1 | (0)1 0 | 1 | 0 | 0.0 (0)1 | (0)1 0.5 | 0 | 0 | 0.0 (0)1 | (0)1 1 | 1 | 0 | 0 (0)1 | |

| '10' ERRATIC DETECTION | | | | | | | | | | | | | | | | | | | | | | |
|------------------------|-------|-------|-------|---|-------|-------|-------|-------------------------|----------|-------|-------|--|----------|-------|-------|-------------------------------|----------|-------|-------|----------|-------|------|
| STEP 55 | | | | STEP 56 | | | | STEP 57 | | | | STEP 58 | | | | STEP 59 | | | | | | |
| G-BLL/R DISCHARGE | | | | G-BLR SELECT PRECHARGE G-BLL PRECHARGE | | | | MEMORY DISCHARGE (VWE1) | | | | SL CLEAR SL SENSE & ALL DETERMINATION | | | | G-BLL/R DISCHARGE SL CLEAR | | | | | | |
| DLL | G-BLL | SL(L) | SL(R) | DLL | G-BLL | SL(L) | SL(R) | DLL | G-BLL | SL(L) | SL(R) | DLL | G-BLL | SL(L) | SL(R) | DLL | G-BLL | SL(L) | SL(R) | G-BLL | G-BLR | DLR |
| (1)0 0 | 1 | 0 | 0 | (0)1 (1)0 | 0.5 | 1 | 0 | 0.0 (0)1 | (1)0 0.5 | 1 | 0 | 0.0 (0)1 | (1)0 0.5 | 1 | 0 | 0.0 (0)1 | (1)0 0.0 | 0 | 0 | 0.0 (0)1 | 0.0 | (0)1 |
| (1)0 0 | 1 | 0 | 0 | (1)0 (1)0 | 0.5 | 1 | 0 | 0.0 (1)0 | (1)0 0.5 | 1 | 0 | 0.0 (1)0 | (1)0 0.5 | 1 | 0 | 0.0 (1)0 | (1)0 0.0 | 0 | 0 | 0.0 (1)0 | 0.0 | (1)0 |
| (0)1 0 | 0 | 1 | 0 | (1)0 (0)1 | 0.5 | 0 | 1 | 0.0 (1)0 | (0)1 0.5 | 0 | 1 | 0.0 (1)0 | (0)1 0.5 | 1 | 0 | 0.0 (1)0 | (0)1 0.0 | 0 | 0 | 0.0 (1)0 | 0.0 | (1)0 |
| (0)1 0 | 1 | 0 | 0 | (0)1 (0)1 | 0.5 | 1 | 0 | 0.0 (0)1 | (0)1 0.5 | 1 | 0 | 0.0 (0)1 | (0)1 0.5 | 1 | 0 | 0.0 (0)1 | (0)1 0.0 | 0 | 0 | 0.0 (0)1 | 0.0 | (0)1 |

ALL DETERMINATION: TO ERASE IF FAIL IS REACHED

FIG. 32

(6) '00' ERRATIC DETECTION

| '00' ERRATIC DATA LATCH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|---|-------|-------|-------|----------|-------|-------|-------|--|-------|-------|-------|---------------------------|-----|-------|-------|-----------------------------|-------|------|-------|----------|-------|-------|------|---|------|------|------|------|
| STEP | STEP 60 | | | | STEP 61 | | | | STEP 62 | | | | STEP 63 | | | | STEP 64 | | | | STEP 65 | | | | | | | | |
| CONTENTS | DATA TRANSFER DLR→G-BLR G-BLL PRECHARGE | | | | SL SENSE | | | | G-BLL/R DISCHARGE DATA TRANSFER SL(L) →G-BLL | | | | OPERATION (DLL, G-BLL) | | | | SL CLEAR G-BLR PRECHARGE | | | | SL SENSE | | | | | | | | |
| | DLL | G-BLL | SL(L) | SL(R) | G-BLL | SL(L) | SL(R) | G-BLL | DLL | G-BLL | SL(L) | SL(R) | G-BLL | DLL | G-BLL | SL(L) | SL(R) | G-BLL | DLL | G-BLL | SL(L) | SL(R) | G-BLL | DLL | | | | | |
| | DLR | G-BLR | SL(R) | SL(L) | G-BLL | SL(R) | SL(L) | G-BLL | DLR | G-BLR | SL(R) | SL(L) | G-BLL | DLR | G-BLR | SL(R) | SL(L) | G-BLL | DLR | G-BLR | SL(R) | SL(L) | G-BLL | DLL | | | | | |
| | (1)0 | 0.5 | | | 0.0 | (0)1 | (1)0 | 1 | 1 | 0 | 0 | (0)1 | (1)0 | 1 | 0 | 0 | (0)1 | (1)0 | 1 | 0 | 0 | (0)1 | (1)0 | 1 | 0 | (0)1 | | | |
| | (1)0 | 0.5 | | | 1.0 | (1)0 | (1)0 | 0 | 0 | 1 | 1 | (1)0 | (1)0 | 0 | 0 | 1 | 0 | (1)0 | (1)0 | 0 | 0 | 0.5 | (1)0 | 0 | 1 | 1 | (1)0 | | |
| 10 | (0)1 | 0.5 | | | 1.0 | (1)0 | (0)1 | 0 | 0 | 1 | 1 | (1)0 | (0)1 | 0 | 0 | 1 | 0 | (1)0 | (0)1 | 1.0 | 0 | 0 | 0.5 | (1)0 | 1 | 1 | 0 | (1)0 | |
| 11 | (0)1 | 0.5 | | | 0.0 | (0)1 | (0)1 | 1 | 1 | 0 | 0 | (0)1 | (0)1 | 1.0 | 1 | 0 | 0 | (0)1 | (0)1 | 1.0 | 0 | 0 | 0.5 | (0)1 | 1 | 1 | 0 | 0 | (0)1 |

| '00' ERRATIC DETECTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------|-------|-------|-------|-------|---|-------|-------|-------|-------|-------------------------|-------|-------|-------|-------|--|-------|-------|-------|-------|-------------------------------|-------|-------|-------|-------|-----|---|---|-----|------|
| STEP 66 | | | | | STEP 67 | | | | | STEP 68 | | | | | STEP 69 | | | | | STEP 70 | | | | | | | | | |
| G-BLL/R DISCHARGE | | | | | G-BLR SELECT PRECHARGE G-BLL PRECHARGE | | | | | MEMORY DISCHARGE (VWE2) | | | | | SL CLEAR SL SENSE & ALL DETERMINATION | | | | | G-BLL/R DISCHARGE SL CLEAR | | | | | | | | | |
| DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLL | | | | |
| (1)0 | 0 | 1 | 0 | 0 | (0)1 | (1)0 | 0.5 | 1 | 0 | 0.0 | (0)1 | (1)0 | 0.5 | 1 | 0 | 0.0 | (0)1 | (1)0 | 0.5 | 1 | 0 | 0.0 | (0)1 | (1)0 | 0.0 | 0 | 0 | 0.0 | (0)1 |
| (1)0 | 0 | 0 | 1 | 0 | (1)0 | (1)0 | 0.5 | 0 | 1 | 1.0 | (1)0 | (1)0 | 0.5 | 0 | 1 | 0.0 | (1)0 | (1)0 | 0.5 | 1 | 0 | 0.0 | (1)0 | (1)0 | 0.0 | 0 | 0 | 0.0 | (1)0 |
| (0)1 | 0 | 1 | 0 | 0 | (1)0 | (0)1 | 0.5 | 1 | 0 | 0.0 | (1)0 | (0)1 | 0.5 | 1 | 0 | 0.0 | (1)0 | (0)1 | 0.5 | 1 | 0 | 0.0 | (1)0 | (0)1 | 0.0 | 0 | 0 | 0.0 | (1)0 |
| (0)1 | 0 | 1 | 0 | 0 | (0)1 | (0)1 | 0.5 | 1 | 0 | 0.0 | (0)1 | (0)1 | 0.5 | 1 | 0 | 0.0 | (0)1 | (0)1 | 0.5 | 1 | 0 | 0.0 | (0)1 | (0)1 | 0.0 | 0 | 0 | 0.0 | (0)1 |

ALL DETERMINATION: TO ERASE IF FAIL IS REACHED

FIG. 34

170. 34

ADDITIONAL WRITE

| STEP | | COMBINATION OF UPPER BITS | | | | | | | | | | | | STEP 19 | | | | | | | | | | | | | |
|----------|----|---------------------------|-------|-------|-------|----------------------------|------|-----|-------|----------|-------|-------|------|-------------------|-------|-------|-------|---|-----|------|-------|---------------------------|-------|-------|-----|---|------|
| | | STEP 14 | | | | STEP 15 | | | | STEP 16 | | | | STEP 17 | | | | STEP 18 | | | | OPERATION (DLL, G-BLL) | | | | | |
| CONTENTS | | G-BLL/R PRECHARGE | | | | MEMORY DISCHARGE (VRW2) | | | | SL SENSE | | | | G-BLL/R DISCHARGE | | | | DATA TRANSFER (SL(L) → G-BLL) G-BLL PRECHARGE | | | | | | | | | |
| | | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | | |
| 01 | 11 | 1(0) | 1 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 1 | 1 | 0(1) | 1(0) | 0 | 0 | 1 | 0 | 0 | 0(1) | 1(0) | 0 | 0 | 1 | 0 | 0 | 0(1) |
| | | 1(0) | 1 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 1 | 1 | 1(0) | 1(0) | 0 | 0 | 1 | 0 | 0 | 1(0) | 1(0) | 0 | 0 | 1 | 0 | 0 | 1(0) |
| | | 1(0) | 1 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 0 | 0 | 1(0) | 1(0) | 1 | 1 | 0 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 0 | 0 | 1(0) |
| | | 0(1) | 1 | 0 | 0 | 0(1) | 0(1) | 1 | 0 | 0 | 0 | 0 | 0(1) | 0(1) | 1 | 1 | 0 | 0 | 0 | 0(1) | 0(1) | 1 | 0 | 0 | 0 | 0 | 0(1) |
| 00 | 11 | 0(1) | 1 | 0 | 0 | 0(1) | 0(1) | 1 | 0 | 0 | 0 | 0 | 1(0) | 0(1) | 1 | 1 | 0 | 0 | 0 | 1(0) | 0(1) | 1 | 0 | 0 | 0 | 0 | 0(1) |
| | | 0(1) | 1 | 0 | 0 | 0(1) | 0(1) | 1 | 0 | 0 | 0 | 0 | 1(0) | 0(1) | 1 | 1 | 0 | 0 | 0 | 1(0) | 0(1) | 1 | 0 | 0 | 0 | 0 | 0(1) |
| | | 1(0) | 1 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 0 | 0 | 1(0) | 1(0) | 1 | 1 | 0 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 0 | 0 | 1(0) |
| | | 1(0) | 1 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 0 | 0 | 1(0) | 1(0) | 1 | 1 | 0 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 0 | 0 | 1(0) |
| 10 | 11 | 1(0) | 1 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 0 | 0 | 0(1) | 1(0) | 1 | 1 | 0 | 0 | 0 | 0(1) | 1(0) | 1 | 0 | 0 | 0 | 0 | 0(1) |
| | | 1(0) | 1 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 0 | 0 | 0(1) | 1(0) | 1 | 1 | 0 | 0 | 0 | 0(1) | 1(0) | 1 | 0 | 0 | 0 | 0 | 0(1) |
| | | 1(0) | 1 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 0 | 0 | 0(1) | 1(0) | 1 | 1 | 0 | 0 | 0 | 0(1) | 1(0) | 1 | 0 | 0 | 0 | 0 | 0(1) |
| | | 1(0) | 1 | 0 | 0 | 1(0) | 1(0) | 1 | 0 | 0 | 0 | 0 | 0(1) | 1(0) | 1 | 1 | 0 | 0 | 0 | 0(1) | 1(0) | 1 | 0 | 0 | 0 | 0 | 0(1) |

(b)

| STEP | | COMBINATION OF UPPER BITS | | | | | | | | | | | | STEP 24 | | | | | | | | | | | | |
|----------|----|---------------------------|-------|-------|-------|----------|-----|-----|-------|-------------------|-------|-------|-----|---------|-------|-------|-------|---------------------------|-----|-----|-------|-------|-------|-------|-----|---|
| | | STEP 20 | | | | STEP 21 | | | | STEP 22 | | | | STEP 23 | | | | WRITE | | | | | | | | |
| CONTENTS | | SL CLEAR DLL CLEAR | | | | DL SENSE | | | | G-BLL/R DISCHARGE | | | | ERASE | | | | TO NORMAL WRITE STEP 2 | | | | | | | | |
| | | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | |
| 01 | 11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 00 | 11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10 | 11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | 11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | |

(b)

FIG. 35

2. ERASE SEQUENCE

| STEP | ERASE VERIFY 1 | | | | | | | | | | | | | | | | | | | | | | | |
|----------|-------------------|-------|-------|-------|-------|-----|-----------------------------|-------|-------|-------|-------|-----|------------------------------|-------|-------|-------|-------|-----|-----------------------------|-------|-------|-------|-------|-----|
| | STEP 1 | | | | | | STEP 2 | | | | | | STEP 3 | | | | | | STEP 4 | | | | | |
| CONTENTS | G-BLL/R PRECHARGE | | | | | | MEMORY DISCHARGE (VEV=2.0V) | | | | | | SL SENSE & ALL DETERMINATION | | | | | | G-BLL/R DISCHARGE, SL CLEAR | | | | | |
| | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR |
| 11 | | 0.5 | | | 1.0 | | | 0.5 | | | 1.0 | | | 0 | 0 | 1 | 1 | | | 0 | 0 | 0 | 0 | |
| BELOW 11 | | 0.5 | | | 1.0 | | | 0.5 | | | 1.0 | | | 0 | 0 | 1 | 1 | | | 0 | 0 | 0 | 0 | |

※ 11: BIT IN WHICH POST-ERASURE V_{th} IS LESS THAN OR EQUAL TO VEV ALL DETERMINATION: ERASE END UPON PASS

BELOW 11: BIT IN WHICH V_{th} OUT OF 11 IS LESS THAN OR EQUAL TO $VWV0$ (BIT INTENDED FOR WRITEBACK)

| ERASE | | | | | | ERASE VERIFY 2 | | | | | | | | | | | | | | | | | |
|--------|-------|-------|-------|-------|-----|----------------------|-------|-------|-------|-------|-----------------------------------|-----|-------|-------|-------|---------------------------------|-----|-----|-------|-------|-------|-------|-----|
| Step 5 | | | | | | Step 6 | | | | | Step 7 | | | | | Step 8 | | | | | | | |
| ERASE | | | | | | G-BLL/R PRECHARGE | | | | | MEMORY DISCHARGE (VEV=2.0V) | | | | | SL SENSE & ALL DETERMINATION | | | | | | | |
| DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR |
| | | | | | | | 0.5 | | | 1.0 | | | 0.5 | | | 0.0 | | | 1 | 1 | 0 | 0 | |
| | | | | | | | 0.5 | | | 1.0 | | | 0.5 | | | 0.0 | | | 1 | 1 | 0 | 0 | |

ALL DETERMINATION: TO STEP 5 UPON FAIL

| | | | | | | '11' ERRATIC DETECTION | | | | | | | | | | | | | | | | | |
|-----------------------------|-------|-------|-------|-------|-----|------------------------|-------|-------|-------|-------|-----|------------------------------|-------|-------|-------|-------|------------------------------|-----|-------|-------|-------|-------|-----|
| Step 9 | | | | | | Step 10 | | | | | | Step 11 | | | | | Step 12 | | | | | | |
| G-BLL/R DISCHARGE, SL CLEAR | | | | | | G-BLL/R PRECHARGE | | | | | | MEMORY DISCHARGE (VWV0=1.2V) | | | | | SL SENSE & ALL DETERMINATION | | | | | | |
| DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR |
| | 0 | 0 | 0 | 0 | | | 0.5 | | | 1.0 | | | 0.5 | | | 1.0 | | | 0 | 0 | 1 | 1 | |
| | 0 | 0 | 0 | 0 | | | 0.5 | | | 1.0 | | | 0.5 | | | 0.0 | | | 1 | 1 | 0 | 0 | |

(a)

ALL DETERMINATION: ERASE END UPON PASS

| WRITE (DEPLETE PREVENTING PROCESS) | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------------|-------|-------|-------|-------|-----|--|-------|-------|-------|-------|-----|------------------------------|-------|-------|-------|-------|-----|--|-------|-------|-------|-------|-----|
| Step 13 | | | | | | Step 14 | | | | | | Step 15 | | | | | | Step 16 | | | | | |
| WRITE | | | | | | G-BLL/R DISCHARGE G-BLL/R PRECHARGE | | | | | | MEMORY DISCHARGE (VWV0=1.2V) | | | | | | SL CLEAR, SL SENSE & ALL DETERMINATION | | | | | |
| DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR |
| | 0.0 | 0.0 | 6.0 | 6.0 | | | 0.5 | 0 | 1 | 1.0 | | | 0.5 | 0 | 1 | 1.0 | | | 0 | 0 | 1 | 1 | |
| | 6.0 | 6.0 | 0.0 | 0.0 | | | 0.5 | 1 | 0 | 1.0 | | | 0.5 | 1 | 0 | 1.0 | | | 0 | 0 | 1 | 1 | |

ALL DETERMINATION: TO STEP 13 UPON FAIL

| '11' ERRATIC DETECTION | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------|-------|-------|-------|-------|-----|-------------------------------|-------|-------|-------|-------|-----|---------------------------------|-------|-------|-------|-------|-----|-----------------------------------|-------|-------|-------|-------|-----|
| Step 17 | | | | | | Step 18 | | | | | | Step 19 | | | | | | Step 20 | | | | | |
| G-BLL/R PRECHARGE | | | | | | MEMORY DISCHARGE (VWDS) | | | | | | SL SENSE & ALL DETERMINATION | | | | | | G-BLL/R DISCHARGE, SL CLEAR | | | | | |
| DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR | DLL | G-BLL | SL(L) | SL(R) | G-BLR | DLR |
| | 0.5 | | | 1.0 | | | 0.5 | | | 0.0 | | | 1 | 1 | 0 | 0 | | | 0 | 0 | 0 | 0 | |
| | 0.5 | | | 1.0 | | | 0.5 | | | 0.0 | | | 1 | 1 | 0 | 0 | | | 0 | 0 | 0 | 0 | |

ALL DETERMINATION: ERASE END UPON PASS

COMBINATION OF LOWER BITS

VRW3 READ

G-BLp PRECHARGE

MEMORY DISCHARGE

SL CLEAR

SL SENSE

OF WL
→ 4.0V)

VCP=7.0V

VRW3=4.0V

VRD1-Vth=1.0V

VRD2-Vth=0.5V

Vth

VSS

VCC

G-BLR

G-BLL

VBCUT-Vth

SLR

SLL

VRD1=1.0V+Vth

VBCUT-Vth

SLP

SLN

VRD1=1.0V+Vth

VSS

VCC

SUPPLY VCC TO RPC

FIG. 37

ADDITIONAL WRITE (LOGIC
COMBINING PROCESS)
OPERATING WAVEFORM

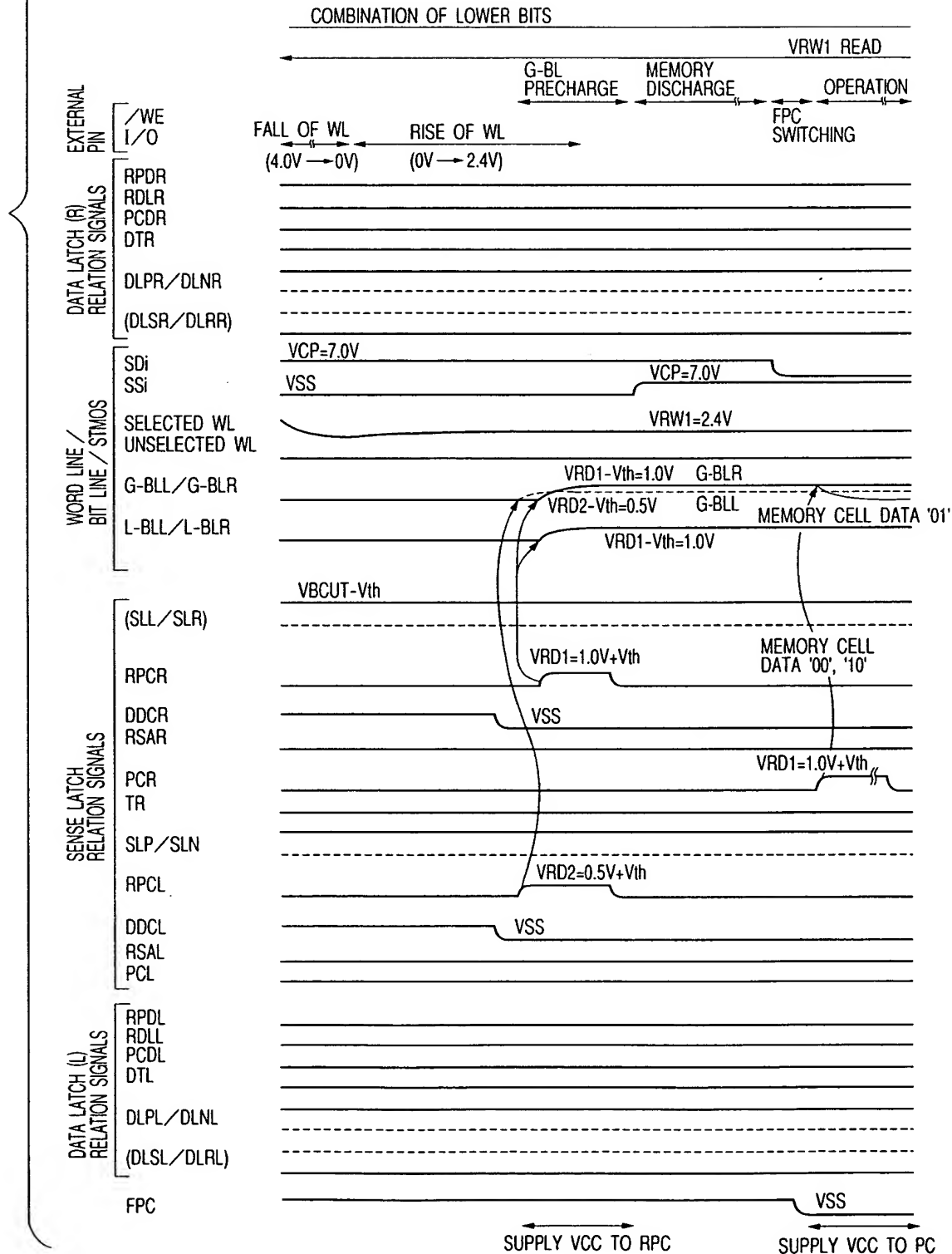
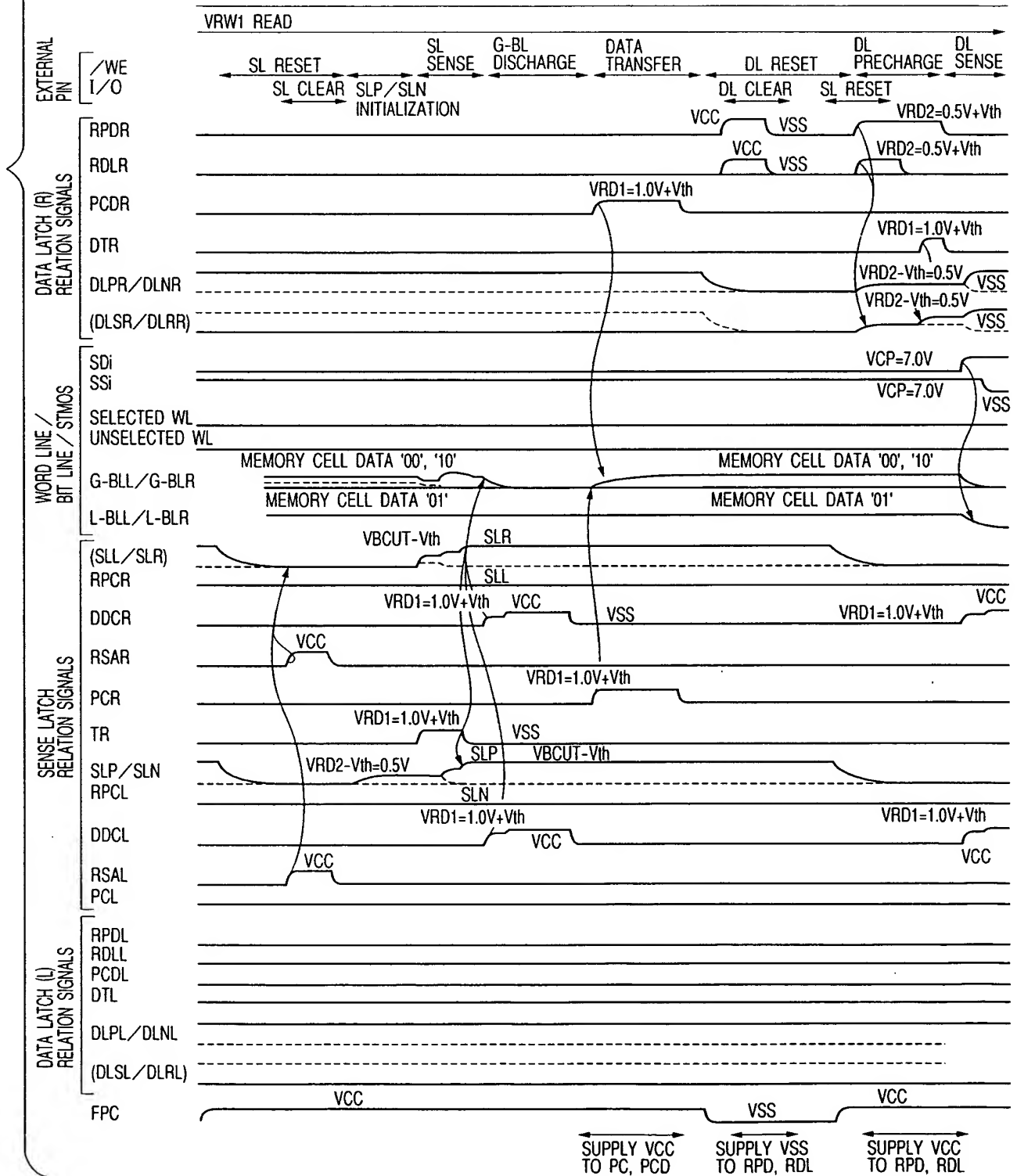


FIG. 38

ADDITIONAL WRITE (LOGIC
COMBINING PROCESS)
OPERATING WAVEFORM



COMBINATION OF UPPER BITS

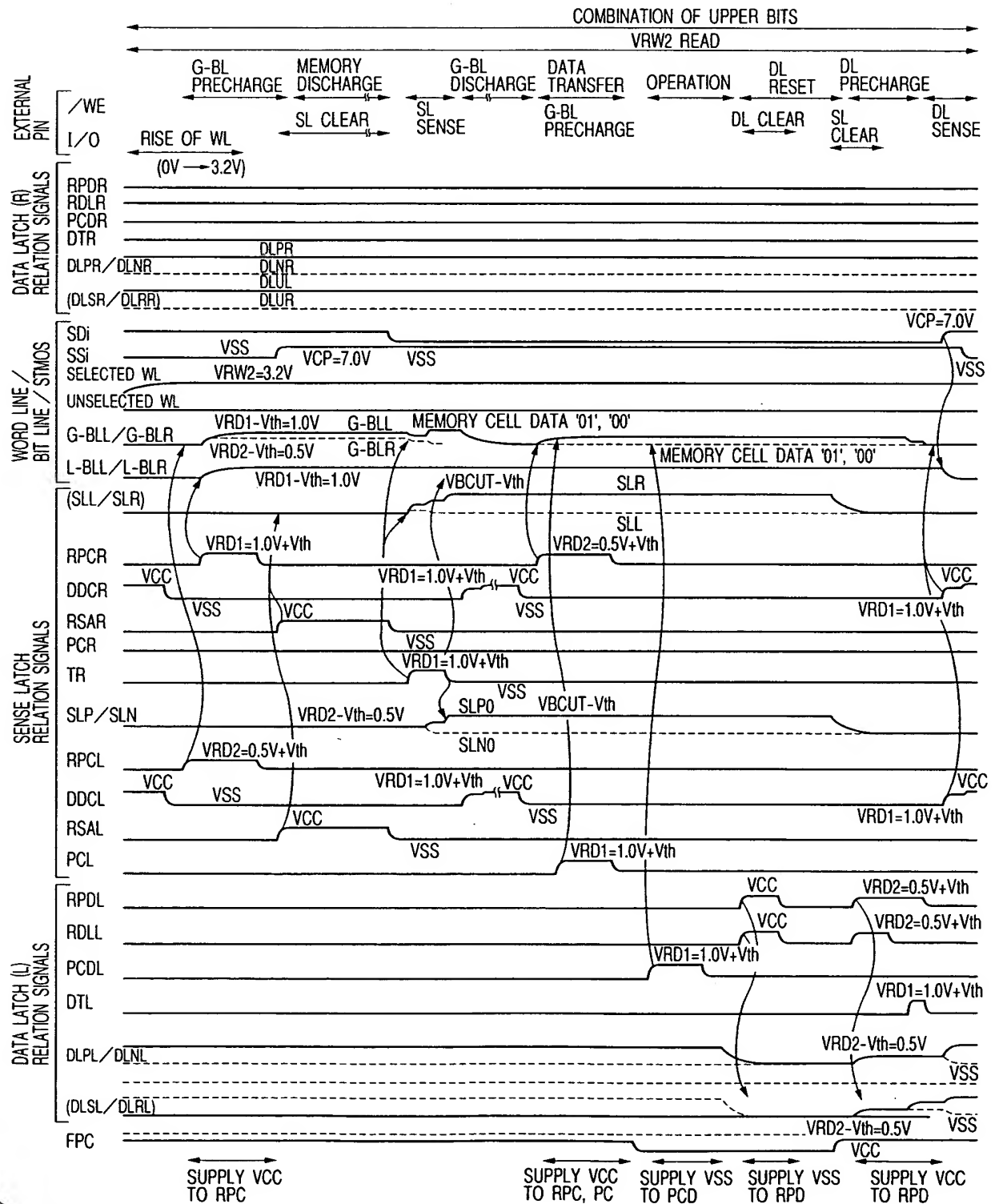


FIG. 40

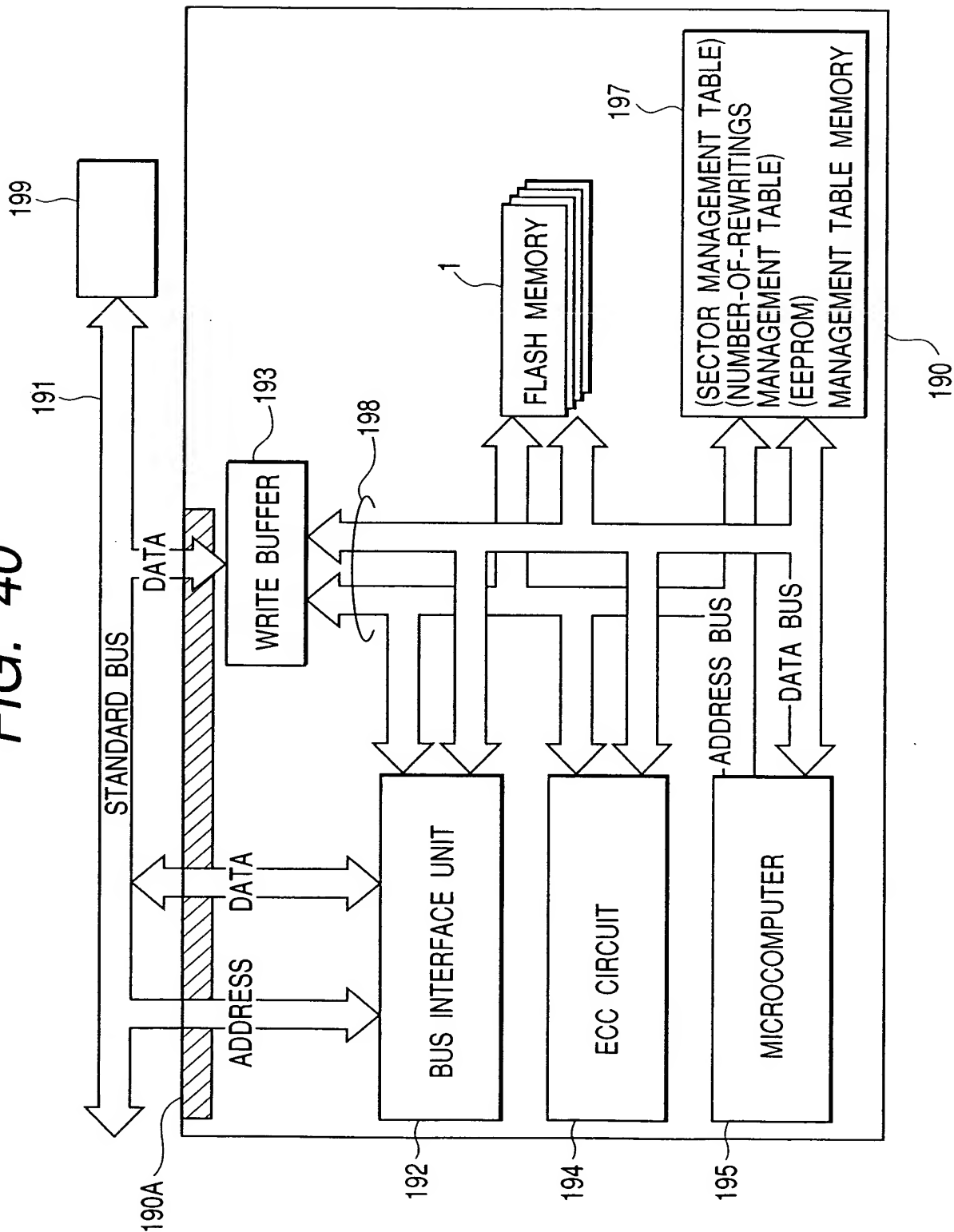


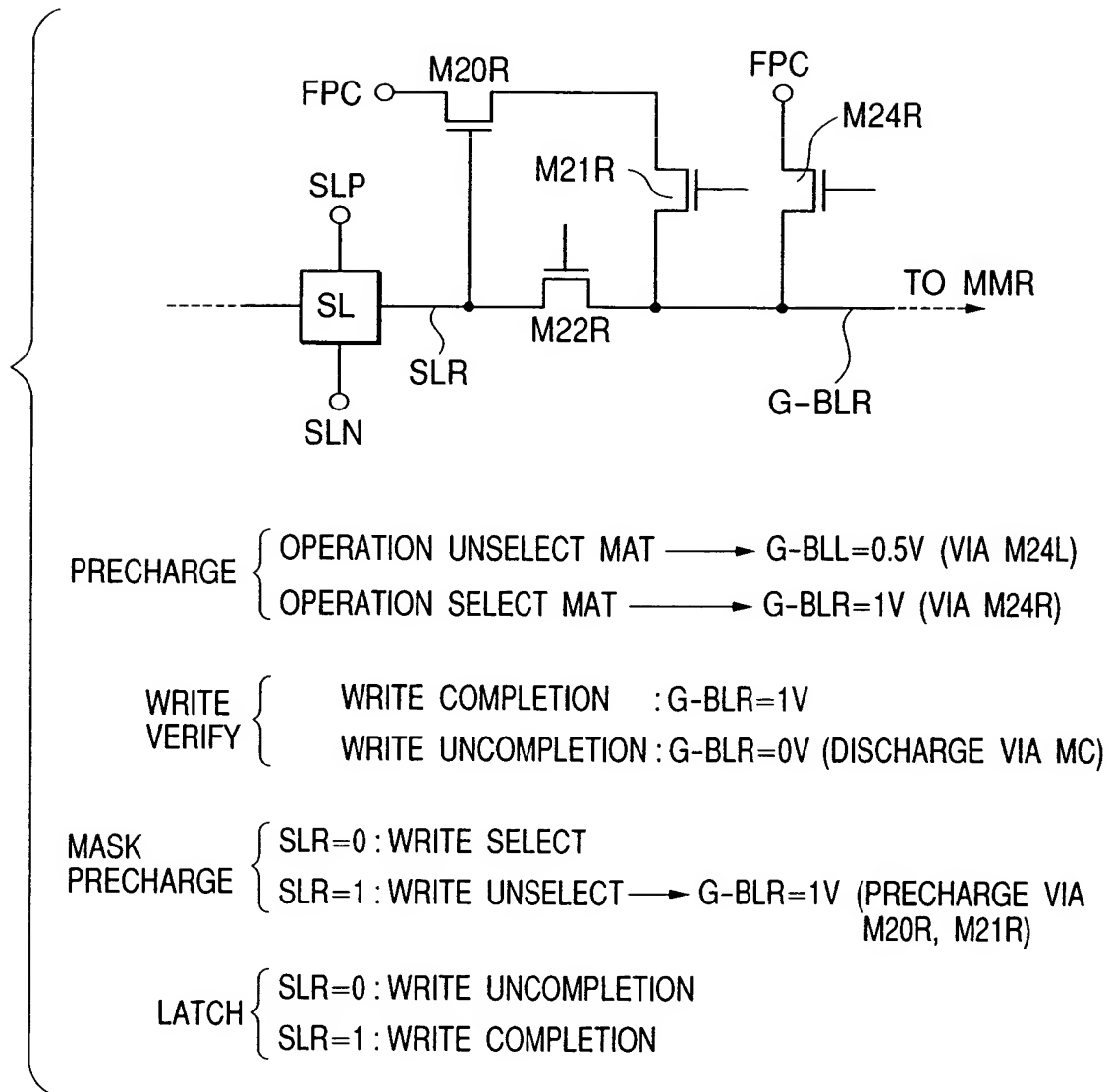
FIG. 41

FIG. 43

SL/DL CIRCUIT LATCH DATA

| WRITE DATA | UPPER DATA I/O4 | LOWER DATA I/O0 | UPON SELECTION OF LEFT MAT | | | UPON SELECTION OF RIGHT MAT | | |
|---------------|-----------------------|-----------------------|-------------------------------|----|-----|--------------------------------|----|-----|
| | | | DLL | SL | DLR | DLL | SL | DLR |
| "01" | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| "00" | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| "10" | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| "11" | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

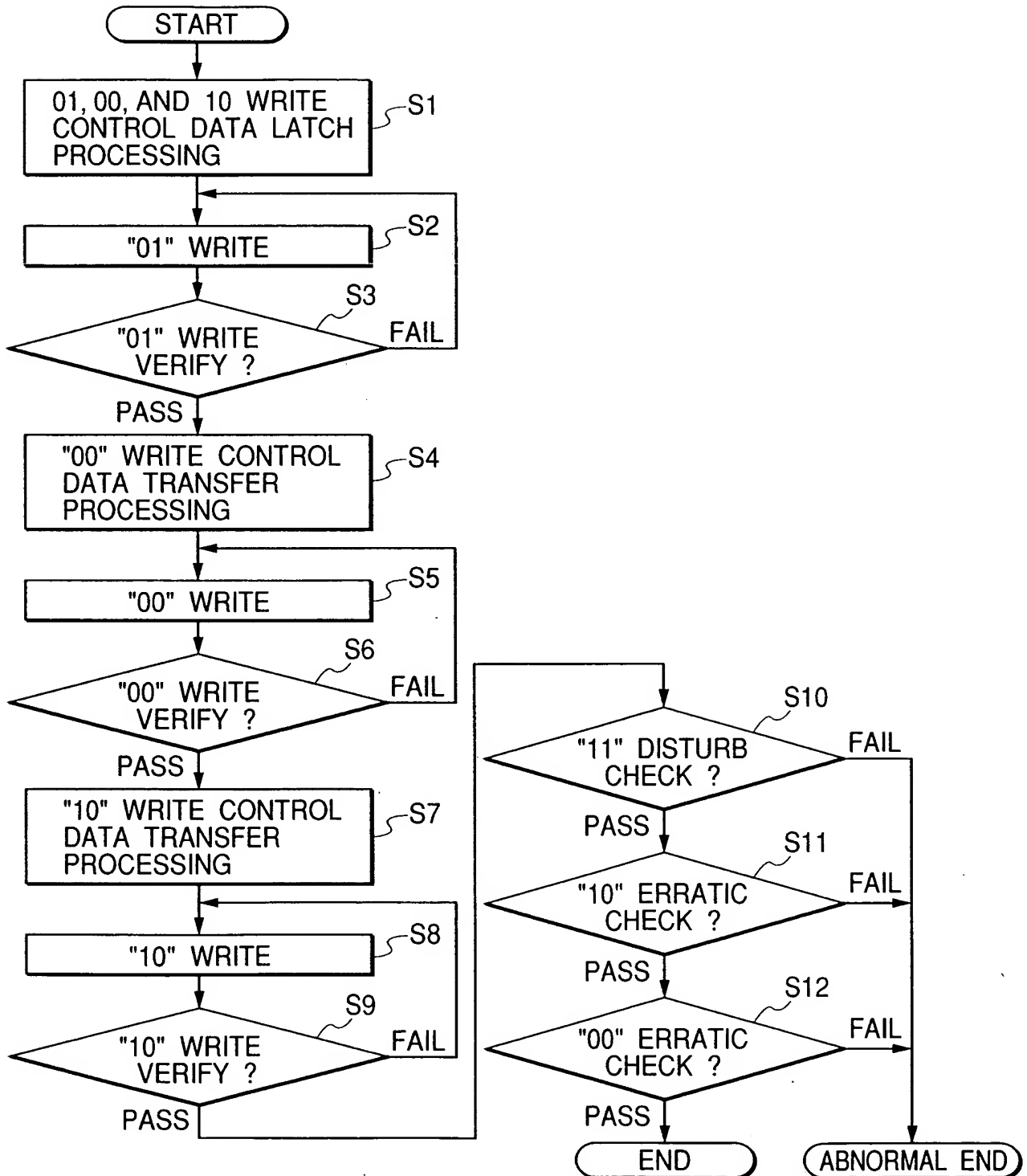
FIG. 44

FIG. 45

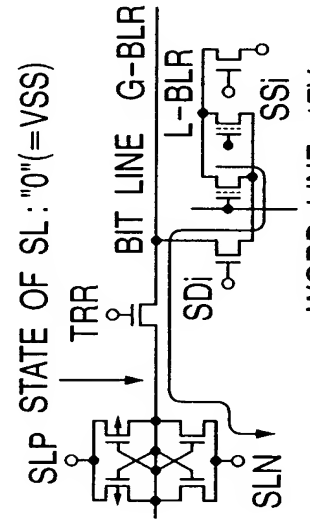
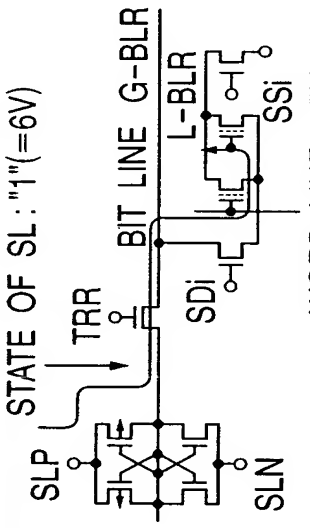
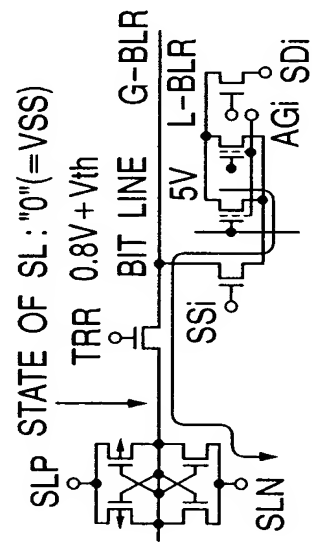
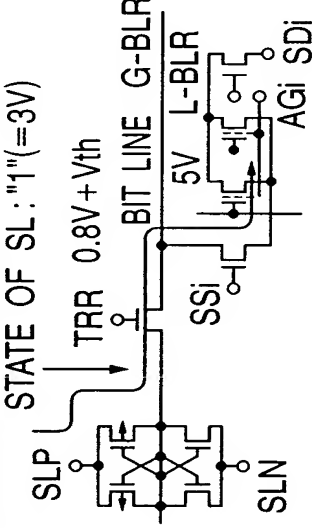
| | WRITE SELECT (SL="0") | WRITE UNSELECT (SL="1") |
|--------------------|--|--|
| AND MEMORY CELL | <p>SLP STATE OF SL : "0" (=VSS)</p>  <p>WORD LINE : 17V</p> <p>MEMORY CELL : $V_{cg}=17V \rightarrow FN$ TUNNEL WRITING</p> | <p>STATE OF SL : "1" (=6V)</p>  <p>WORD LINE : 17V</p> <p>MEMORY CELL : $V_{cg}=11V \rightarrow$ WRITE UNSELECTION</p> |
| AG-AND MEMORY CELL | <p>SLP STATE OF SL : "0" (=VSS)</p>  <p>WORD LINE : 17V AG : 0.6V</p> <p>MEMORY CELL : $V_{ds}=5V \rightarrow HC$ WRITE</p> | <p>STATE OF SL : "1" (=3V)</p>  <p>WORD LINE : 17V AG : 0.6V</p> <p>MEMORY CELL : $V_{ds}=0V$ (AG : CUT OFF) \rightarrow WRITE UNSELECTION</p> |

FIG. 46
("11" DISTURB CHECK)

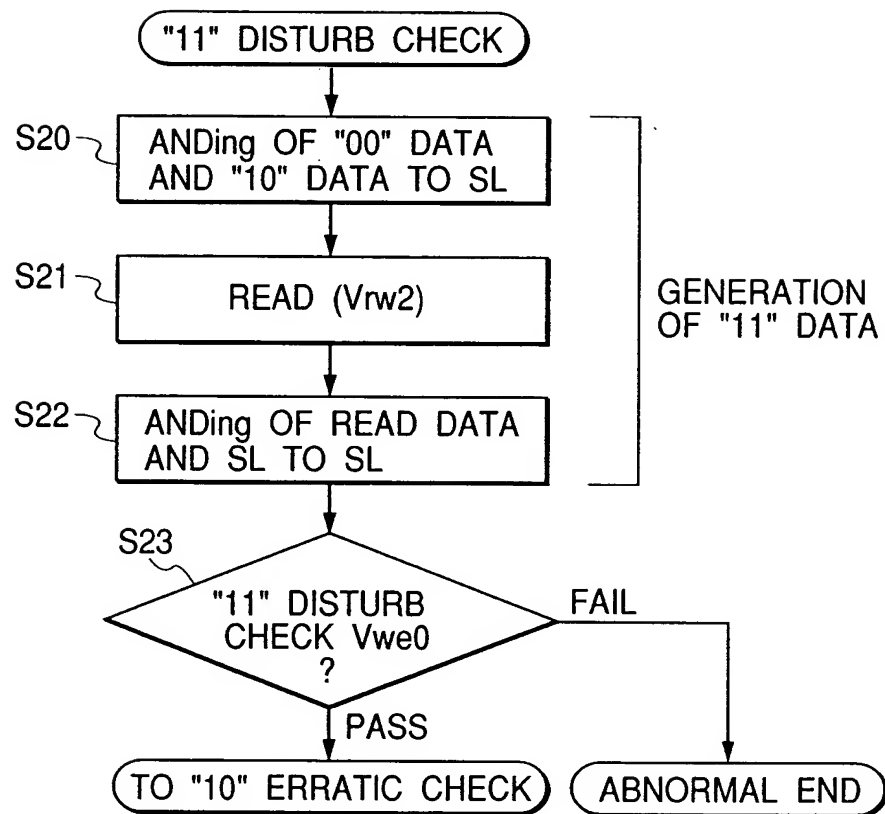


FIG. 47

(GENERATION OF "11" DATA)

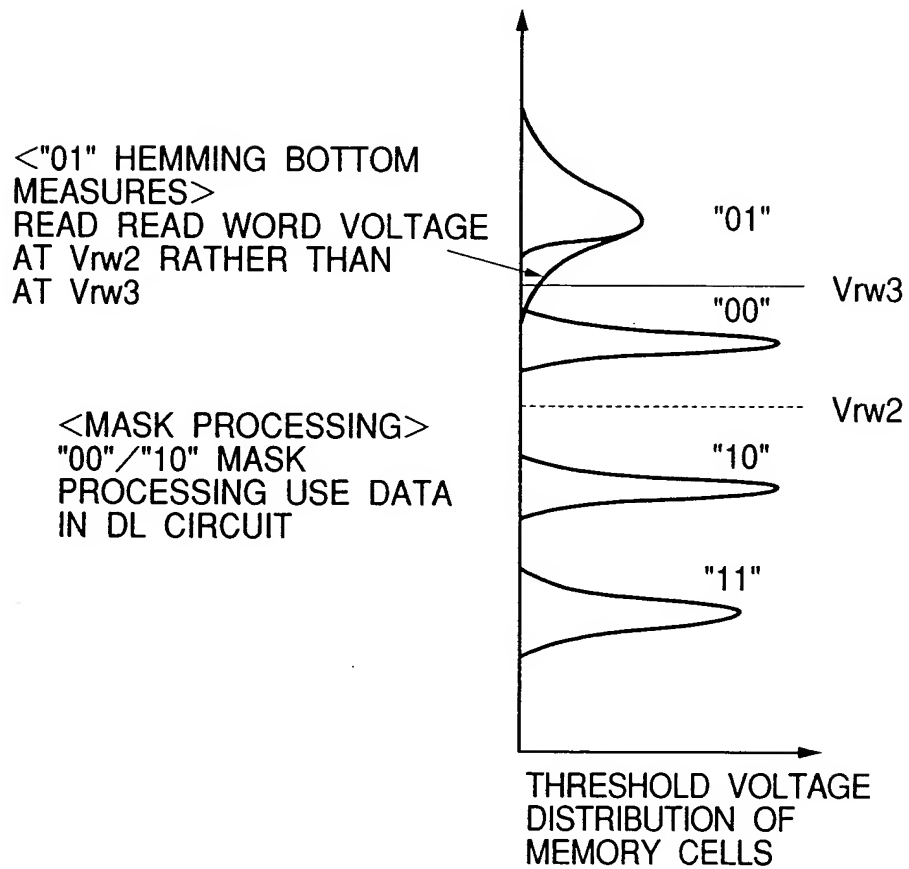


FIG. 48

(4) "11" DISTURB CHECK

| WRITE DATA | "11" DISTURB CHECK | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|-----------------------------|-------|-------|-------|-------|-------|------------------------------------|-------|-------|-------|-------|-------|---------------------------|-------|-------|-------|-------|-------|----------|-------|-------|-------|-------|-------|---|
| | STEP 30 | | | | | | STEP 31 | | | | | | STEP 32 | | | | | | STEP 33 | | | | | | |
| | SL CLEAR BL(L)/(R) CLEAR | | | | | | BL(R) PRECHARGE BL(L) PRECHARGE | | | | | | DL(R) SELECT DISCHARGE | | | | | | SL SENSE | | | | | | |
| | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | |
| "01" | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.5 | 0 | 0 | 1 | 1 | 0 | 0.5 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| "00" | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0.5 | 0 | 0 | 1 | 1 | 1 | 0.5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| "10" | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.5 | 0 | 0 | 1 | 0 | 0 | 0.5 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| "11" | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.5 | 0 | 0 | 1 | 1 | 0 | 0.5 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

| STEP 34 | | | | | | STEP 35 | | | | | | STEP 36 | | | | | | STEP 37 | | | | | |
|---|-------|-------|-------|-------|-------|-----------------|-------|-------|-------|-------|-------|----------------------|-------|-------|-------|-------|-------|---------------------|-------|-------|-------|-------|-------|
| DL(L) SELECT DISCHARGE BL(R) DISCHARGE | | | | | | BL(R) PRECHARGE | | | | | | SL CLEAR SL SENSE | | | | | | BL(L)/(R) DISCHARGE | | | | | |
| DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0.5 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0.5 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0.5 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0.5 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

| STEP 38 | | | | | | STEP 39 | | | | | | STEP 40 | | | | | | STEP 41 | | | | | |
|---------------------|-------|-------|-------|-------|-------|---------------------------|-------|-------|-------|-------|-------|---------------------------|-------|-------|-------|-------|-------|----------|-------|-------|-------|-------|-------|
| BL(L)/(R) PRECHARGE | | | | | | MEMORY DISCHARGE (Vw2) | | | | | | BL(R) SELECT PRECHARGE | | | | | | SL SENSE | | | | | |
| DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) |
| 0 | 0.5 | 1 | 0 | 0 | 1 | 0 | 0.5 | 1 | 0 | 1 | 1 | 0 | 0.5 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0.5 | 0 | 1 | 0 | 1 | 1 | 0.5 | 0 | 1 | 1 | 1 | 1 | 0.5 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0.5 | 0 | 1 | 0 | 0 | 0 | 0.5 | 0 | 1 | 0 | 0 | 0 | 0.5 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0.5 | 1 | 0 | 0 | 1 | 0 | 0.5 | 1 | 0 | 0 | 1 | 0 | 0.5 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

| STEP 42 | | | | | | STEP 43 | | | | | | STEP 44 | | | | | | STEP 45 | | | | | |
|--|-------|-------|-------|-------|-------|---------------------------|-------|-------|-------|-------|-------|----------------------------|-------|-------|-------|-------|-------|-------------------------------|-------|-------|-------|-------|-------|
| BL(L)/(R) DISCHARGE BL(L)/(R) PRECHARGE | | | | | | BL(R) SELECT DISCHARGE | | | | | | MEMORY DISCHARGE (Vwe0) | | | | | | SL SENSE ALL DETERMINATION | | | | | |
| DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) |
| 0 | 0.5 | 0 | 1 | 0 | 1 | 0 | 0.5 | 0 | 1 | 0 | 1 | 0 | 0.5 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0.5 | 0 | 1 | 0 | 1 | 1 | 0.5 | 0 | 1 | 0 | 1 | 1 | 0.5 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0.5 | 0 | 1 | 0 | 0 | 0 | 0.5 | 0 | 1 | 0 | 0 | 0 | 0.5 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0.5 | 1 | 0 | 0 | 1 | 0 | 0.5 | 1 | 0 | 1 | 1 | 0 | 0.5 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

▲ IN THE CASE OF PASS

FIG. 49
(RESTORATION OF "01" DATA)

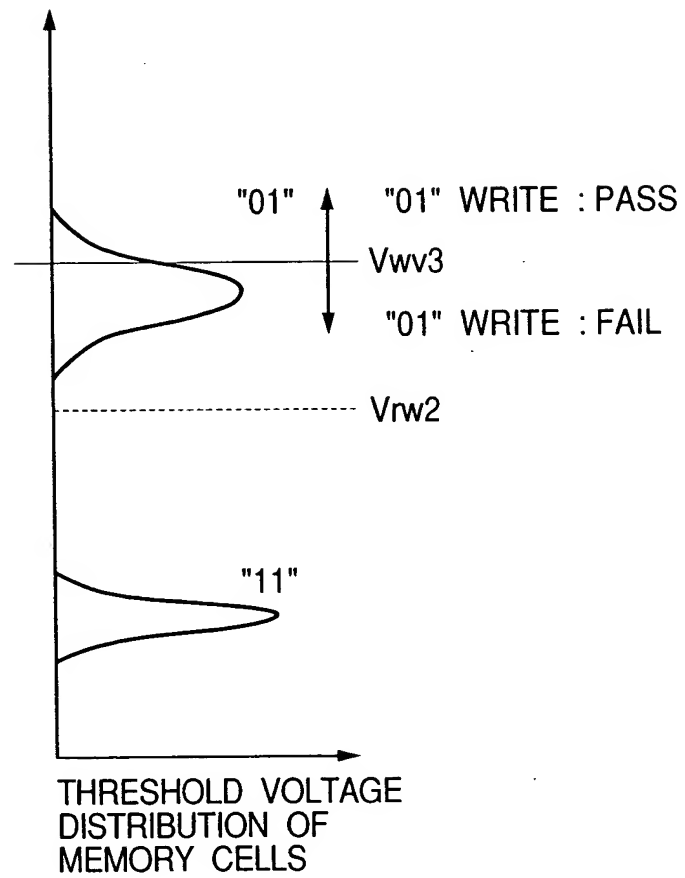


FIG. 50

(PROGRAM RETRY)

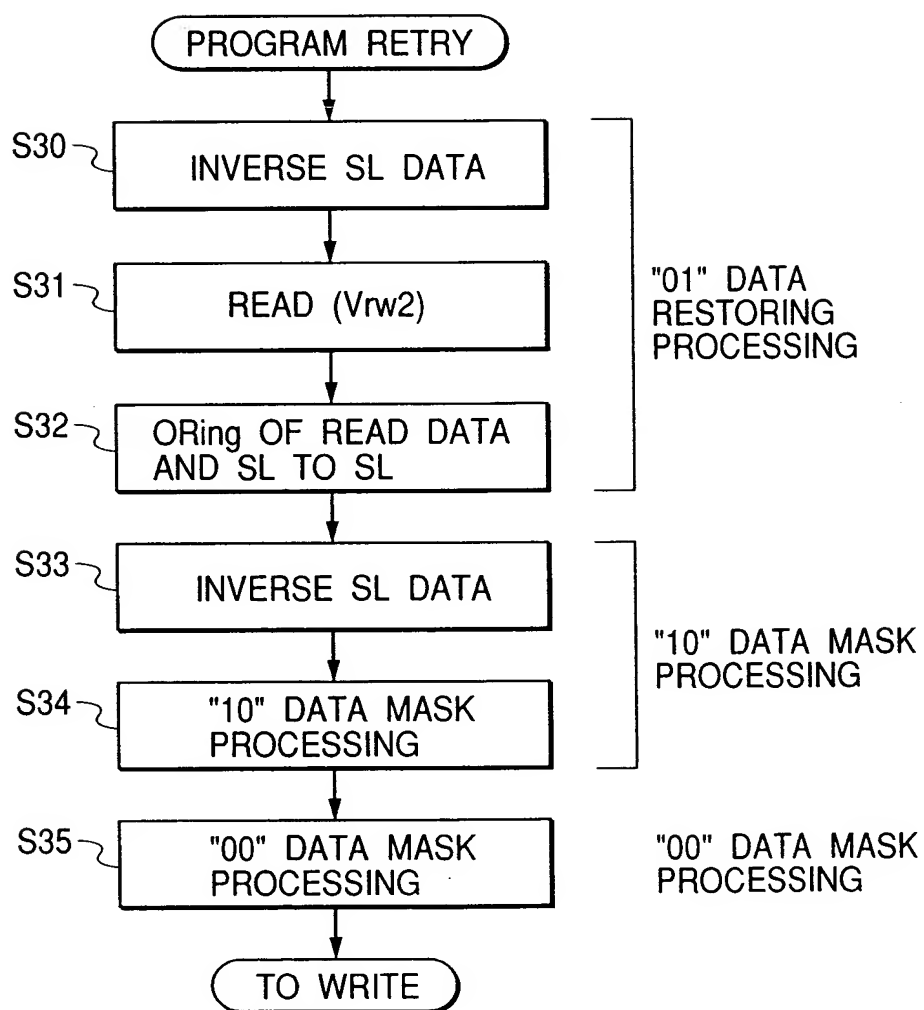


FIG. 51

(PROGRAM RETRY)
(1) DATA RESTORING PROCESSING

| INITIAL STATE | | '01' DATA RESTORING PROCESSING + "11" DATA MASK PROCESSING | | | | | | | | | | | | | | | | | | | | | |
|---------------|--|--|-------|-------|----------------------|-------|-------|-------|------------------------|-------|-------|-------|-------------------|-------|-------|-------|----------------------|-------|-------|-------|-------|-------|---|
| | | SL INVERSION | | | | | | | | | | | | | | | | | | | | | |
| WRITE DATA | STEP 0 | | | | STEP 1 | | | | STEP 2 | | | | STEP 3 | | | | STEP 4 | | | | | | |
| | STATE OF ON-"01" WRITE ABNORMAL COMPLETION | | | | BL(L)/ (R) PRECHARGE | | | | SELECT DISCHARGE SL(R) | | | | SL CLEAR SL SENSE | | | | BL(L)/ (R) DISCHARGE | | | | | | |
| | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | BL(R) | SL(R) | SL(L) | DL(L) | |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0.4 | 1 | 0 | 0.7 | 1 | 0 | 0.4 | 1 | 0 | 0.7 | 1 | 0 | 0.7 | 1 | 0 | 0 |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0.4 | 0 | 1 | 0.7 | 1 | 0 | 0.4 | 0 | 1 | 0.7 | 1 | 0 | 0.7 | 1 | 0 | 0 |
| | | 1 | 0 | 1 | 1 | 1 | 0.4 | 0 | 1 | 0.7 | 1 | 1 | 0.4 | 0 | 1 | 0.7 | 1 | 1 | 0.4 | 0 | 1 | 0 | 1 |
| | | 0 | 0 | 1 | 0 | 0 | 0.4 | 0 | 1 | 0.7 | 0 | 0 | 0.4 | 0 | 1 | 0.7 | 1 | 0 | 0.4 | 0 | 1 | 0 | 0 |
| | | 0 | 0 | 1 | 1 | 1 | 0 | 0.4 | 0 | 1 | 0.7 | 1 | 0 | 0.4 | 0 | 1 | 0.7 | 1 | 0 | 0.4 | 0 | 1 | 0 |
| "01" | FAIL | 0 | 0 | 1 | 0 | 1 | 0 | 0.4 | 1 | 0 | 0.7 | 1 | 0 | 0.4 | 1 | 0 | 0.7 | 1 | 0 | 0.7 | 1 | 0 | 1 |
| | PASS | 0 | 0 | 0 | 1 | 1 | 0 | 0.4 | 0 | 1 | 0.7 | 1 | 0 | 0.4 | 0 | 1 | 0.7 | 1 | 0 | 0.7 | 1 | 0 | 1 |
| "00" | | | | | | | | | | | | | | | | | | | | | | | |
| "10" | | | | | | | | | | | | | | | | | | | | | | | |
| "11" | | | | | | | | | | | | | | | | | | | | | | | |

▲ GUARANTEE ONLY DL IN INITIAL STAGE

| "41" DATA MASK PROCESSING | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|-------------------------------------|-------|-------|-------|-------|-------|-------|-------|---------------------------|-------|-------|-------|-------|-------|-------|-------|----------------------|-------|-------|-------|-------|-------|---|--|---------------------|--|--|--|--|--|--|--|
| STEP 5 | | | | | | | | STEP 6 | | | | | | | | STEP 7 | | | | | | | | STEP 8 | | | | | | | | STEP 9 | | | | | | | |
| BL(L)/(R) PRECHARGE | | | | | | | | MEMORY DISCHARGE V _{W2} | | | | | | | | SELECT PRECHARGE SL(R) | | | | | | | | SL CLEAR SL SENSE | | | | | | | | BL(L)/(R) DISCHARGE | | | | | | | |
| DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | | | | | | | | | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | | | | | | | | | |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | | | | | | | | | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | | | | | | | | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | | | | | | | | |

▲ "01" FAIL MEANS THAT V_{th} STATE IS DIVIDED WITH V_{w2} AS BORDER

▲ MASK "01" FAIL

FIG. 52

| "10" DATA MASK PROCESSING | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|------|---------------------|-------|-------|-------|------------------------|-------|-------|-------|-------------------|-------|-------|-------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| WRITE DATA | | STEP 10 | | | | STEP 11 | | | | STEP 12 | | | | STEP 13 | | | | | | | | |
| | | SL INVERSION | | | | BL(R) SELECT DISCHARGE | | | | SL CLEAR SL SENSE | | | | BL(L)/(R) DISCHARGE | | | | | | | | |
| | | BL(L)/(R) PRECHARGE | | | | DL(R) | | | | DL(L) | | | | DL(R) | | | | DL(L) | | | | |
| | | DL(L) | SL(L) | SL(R) | BL(R) | DL(L) | SL(L) | SL(R) | BL(R) | DL(L) | SL(L) | SL(R) | BL(R) | DL(L) | SL(L) | SL(R) | BL(R) | DL(L) | SL(L) | SL(R) | BL(R) | DL(R) |
| "01" | FAIL | 0 | 0.4 | 0 | 1 | 0 | 0.4 | 0 | 1 | 0 | 0.4 | 0 | 1 | 0 | 0.4 | 0 | 1 | 0 | 0.4 | 0 | 1 | |
| "01" | PASS | 0 | 0.4 | 0 | 1 | 0 | 0.4 | 0 | 1 | 0 | 0.4 | 0 | 1 | 0 | 0.4 | 0 | 1 | 0 | 0.4 | 0 | 1 | |
| "00" | | 1 | 0/1 | 0/1 | 1/0 | 0 | 1 | 0.4 | 0/1 | 1/0 | 0 | 1 | 0.4 | 0/1 | 1/0 | 0 | 1 | 0.4 | 0/1 | 1/0 | 0 | 1 |
| "10" | | 0 | 0.4 | 0/1 | 1/0 | 0 | 0 | 0.4 | 0/1 | 1/0 | 0 | 0 | 0.4 | 0/1 | 1/0 | 0 | 0 | 0.4 | 0/1 | 1/0 | 0 | |
| "11" | | 0 | 0.4 | 1 | 0 | 0 | 1 | 0 | 0.4 | 1 | 0 | 0.7 | 1 | 0 | 0 | 0.7 | 1 | 0 | 0 | 0 | 1 | |

▲ VALUE OF SL VARIES ACCORDING TO Vth STATE UPON "00" AND "10" WRITE ABNORMAL END AFTER STEP 10, DESCRIBE "00" AND "10" ABNORMAL END IN CONSIDERATION THEREOF

| "10" DATA MASK PROCESSING | | | | | | | | | | | | | | | | | | | | |
|---------------------------|-------|-------|-------|------------------------------|-------|-------|-------|------------------------------|-------|-------|-------|-------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| STEP 14 | | | | STEP 15 | | | | STEP 16 | | | | STEP 17 | | | | | | | | |
| BL(L)/(R) PRECHARGE | | | | BL(R) SELECT DISCHARGE DL(R) | | | | BL(R) SELECT PRECHARGE SL(R) | | | | SL CLEAR SL SENSE | | | | | | | | |
| DL(L) | SL(L) | SL(R) | BL(R) | DL(L) | SL(L) | SL(R) | BL(R) | DL(L) | SL(L) | SL(R) | BL(R) | DL(L) | SL(L) | SL(R) | BL(R) | DL(L) | SL(L) | SL(R) | BL(R) | DL(R) |
| 0 | 1 | 0 | 0 | 1 | 0 | 0.4 | 1 | 0 | 0.4 | 1 | 0 | 0 | 0.4 | 1 | 0 | 0 | 0.4 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0.4 | 1 | 0 | 0.4 | 1 | 0 | 0 | 0.4 | 1 | 0 | 0 | 0.4 | 1 | 0 | 0 |
| 1 | 1/0 | 0/1 | 0 | 1 | 0.4 | 1/0 | 0/1 | 0 | 1 | 0.4 | 1/0 | 0/1 | 0 | 1 | 0.4 | 1/0 | 0/1 | 0 | 1 | 0 |
| 0 | 1/0 | 0/1 | 0 | 0 | 0.4 | 1/0 | 0/1 | 0.7 | 0 | 0 | 0.4 | 1/0 | 0/1 | 0.7 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0.4 | 0 | 1 | 0 | 0.4 | 0 | 1 | 0 | 0.4 | 0 | 1 | 0 | 0 | 0 | 1 |

| "00" DATA MASK PROCESSING | | | | | | | | | | | | | | | | | | | |
|--|-------|-------|-------|-----------------|-------|-------|-------|-------------------|-------|-------|-------|-------|-------|--|--|--|--|--|--|
| STEP 18 | | | | STEP 19 | | | | STEP 20 | | | | | | | | | | | |
| BL(L) SELECT DISCHARGE BL(R) DISCHARGE | | | | BL(R) PRECHARGE | | | | SL CLEAR SL SENSE | | | | | | | | | | | |
| DL(L) | SL(L) | SL(R) | BL(R) | DL(L) | SL(L) | SL(R) | BL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | | | | | | |
| 0 | 0.7 | 1 | 0 | 0 | 1 | 0 | 0.7 | 1 | 0 | 0.7 | 1 | 0 | 0 | | | | | | |
| 0 | 0.7 | 1 | 0 | 0 | 1 | 0 | 0.7 | 1 | 0 | 0.7 | 1 | 0 | 0 | | | | | | |
| 1 | 1/0 | 0/1 | 0 | 1 | 0 | 1/0 | 0/1 | 0 | 1 | 0 | 0 | 0 | 0 | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | |

FIG. 53

(DATA RECOVERY READ)

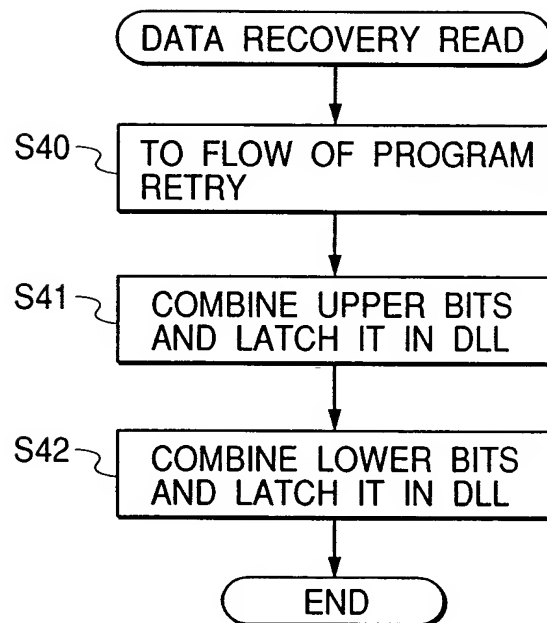


FIG. 54

(DATA RECOVERY READ)

| WRITE DATA | DATA LATCH PROCESSING (COMBINATION OF UPPER BITS) | | | | | | | | | | | | | | | | | | | | | | | |
|------------|---|-------|-------|-------|-------|-------|-----------------|-------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|-------|
| | STEP 0 | | | | | | STEP 1 | | | | | | STEP 2 | | | | | | STEP 3 | | | | | |
| | INITIAL DATA | | | | | | BL(L) PRECHARGE | | | | | | BL(L) SELECT DISCHARGE DL(L) | | | | | | BL(L) SELECT DISCHARGE SL(L) | | | | | |
| | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) |

| | | | | | | | | | | | | | | | | | | | | | | | | |
|------|---|--|---|---|--|---|---|-----|---|---|--|---|---|-----|---|---|--|---|---|-----|---|---|--|---|
| "01" | 0 | | 1 | 0 | | 1 | 0 | 1.2 | 1 | 0 | | 1 | 0 | 1.2 | 1 | 0 | | 1 | 0 | 0 | 1 | 0 | | 1 |
| "00" | 1 | | 0 | 1 | | 1 | 1 | 1.2 | 0 | 1 | | 1 | 1 | 0 | 0 | 1 | | 1 | 1 | 0 | 0 | 1 | | 1 |
| "10" | 0 | | 0 | 1 | | 0 | 0 | 1.2 | 0 | 1 | | 0 | 0 | 1.2 | 0 | 1 | | 0 | 0 | 1.2 | 0 | 1 | | 0 |
| "11" | 0 | | 0 | 1 | | 1 | 0 | 1.2 | 0 | 1 | | 1 | 0 | 1.2 | 0 | 1 | | 1 | 0 | 1.2 | 0 | 1 | | 1 |

▲ AFTER COMPLETION OF PROGRAM RETRY DATA LATCH

| STEP 4 | | | | | | STEP 5 | | | | | |
|----------------------------|-------|-------|-------|-------|-------|-----------------|-------|-------|-------|-------|-------|
| DL(L) CLEAR DL(L) SENSE | | | | | | BL(L) DISCHARGE | | | | | |
| DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) |

| | | | | | | | | | | | |
|---|-----|---|---|--|---|---|---|---|---|--|---|
| 0 | 0 | 1 | 0 | | 1 | 0 | 0 | 1 | 0 | | 1 |
| 0 | 0 | 0 | 1 | | 1 | 0 | 0 | 0 | 1 | | 1 |
| 1 | 1.2 | 0 | 1 | | 0 | 1 | 0 | 0 | 1 | | 0 |
| 1 | 1.2 | 0 | 1 | | 1 | 1 | 0 | 0 | 1 | | 1 |

▲ DETERMINATION OF UPPER BIT

| (COMBINATION OF LOWER BITS) | | | | | | | | | | | | | | | | | | | | | | | |
|---|-------|-------|-------|-------|-------|-----------------|-------|-------|-------|-------|-------|----------------------|-------|-------|-------|-------|-------|---------------------|-------|-------|-------|-------|-------|
| STEP 6 | | | | | | STEP 7 | | | | | | STEP 8 | | | | | | STEP 9 | | | | | |
| BL(L) SELECT PRECHARGE DL(L) & SL(L) | | | | | | BL(R) PRECHARGE | | | | | | SL CLEAR SL SENSE | | | | | | BL(L)/(R) DISCHARGE | | | | | |
| DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) |

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|-----|---|---|--|---|---|-----|---|---|-----|---|---|-----|-----|-----|-----|---|---|---|---|---|---|---|
| 0 | 0.7 | 1 | 0 | | 1 | 0 | 0.7 | 1 | 0 | 0.4 | 1 | 0 | 0.7 | 0.7 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | | 1 | 0 | 0 | 0 | 1 | 0.4 | 1 | 0 | 0 | 0 | 0.4 | 0.4 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0.7 | 0 | 1 | | 0 | 1 | 0.7 | 0 | 1 | 0.4 | 0 | 1 | 0.7 | 0.7 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0.7 | 0 | 1 | | 1 | 1 | 0.7 | 0 | 1 | 0.4 | 1 | 1 | 0.7 | 0.7 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

| STEP 10 | | | | | | STEP 11 | | | | | | STEP 12 | | | | | | STEP 13 | | | | | |
|-----------------|-------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|-------|----------------------------|-------|-------|-------|-------|-------|
| BL(R) PRECHARGE | | | | | | BL(R) SELECT DISCHARGE DL(R) | | | | | | BL(R) SELECT PRECHARGE SL(R) | | | | | | DL(R) CLEAR DL(R) SENSE | | | | | |
| DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) | DL(L) | BL(L) | SL(L) | SL(R) | BL(R) | DL(R) |

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|-----|---|---|---|---|---|-----|---|---|---|---|---|-----|-----|---|---|---|---|-----|-----|
| 0 | 0 | 1 | 0 | 1.2 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1.2 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.2 | 1 | 0 | 0 | 0 | 1 | 1.2 |
| 1 | 0 | 1 | 0 | 1.2 | 0 | 1 | 0 | 1 | 0 | 1.2 | 0 | 1 | 0 | 1 | 0 | 1.2 | 0 | 1 | 0 | 1 | 0 | 1.2 | 1 |
| 1 | 0 | 1 | 0 | 1.2 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

▲ DETERMINATION OF LOWER BIT

FIG. 55

